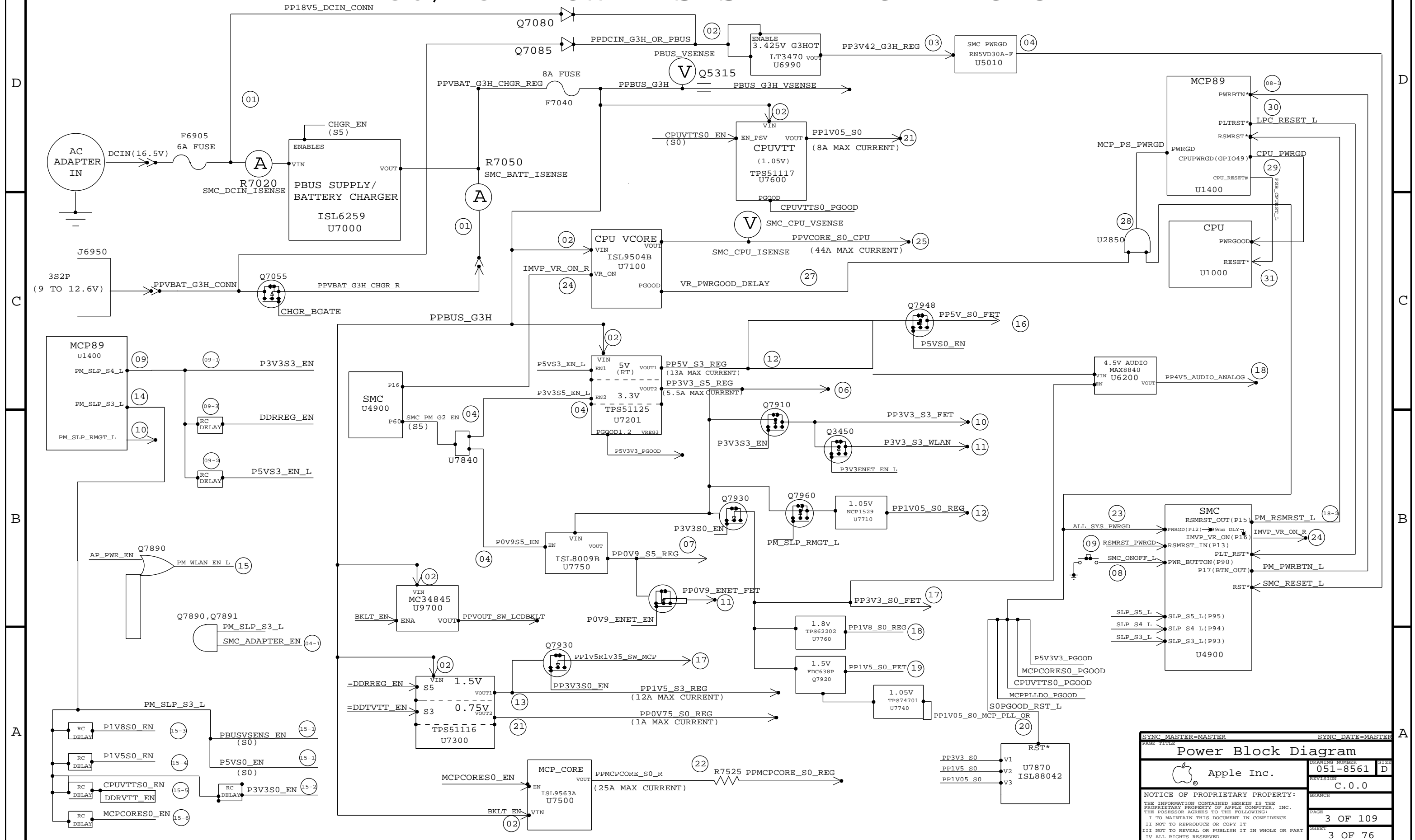



K86/K87 POWER SYSTEM ARCHITECTURE



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	<div>Revision History</div> <div>NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.</div> <div>10/1/2009:INITIAL RELEASE 0.0.1- - ALL PAGES SYNC'ED FROM K84 - REPLACED K84 MCP AND CPU PAGES WITH K6 PAGES - UPDATED SCHEMATIC AND PCB PART NUMBER INFO</div> <div>2009-12-03: Proto 0 release 1.0.0</div> <div>2009-12-04: 1.1.0 csa 3: Updated CPU block text to include CPU description for both K86 and K87 csa 3: Updated text note to include K86 in title csa 4: Added BOM entry under Module Parts table to include CULV processor (337S3779) to minimize delta on this page between K86 and K87 per Diana</div> <div>2009-12-07: 1.2.0 csa 74: Component value changes per Leo (Intersil): R7417 from 5.36k => 6.34k, 1% (11450395) C7417 from 0.12uF to 0.22uF (13250102) Implemented different stuffing options for 1-phase vs 2-phase: Added IMVP6:2PHASE to the following components: R7417, C7428, R7409, R7411, C7406, R7414, C7414, C7413 Added BOM table to insert the following APNs for IMVP6:1PHASE: R7417 = 7.68K 1% (11450304) C7428 = 0.22uF 10% (13250102) R7409 = 5.9K 1% (13250256) R7411 = 25% 1% (11450160) C7406 = 4700pF 10% (13250720) R7414 = 97.5K 1% (11450410) C7414 = 1000pF 10% (13250045) C7413 = 100uF 5% (131S1027) Updated table to add new values for lphase (PWM freq., Max current, Load line) csa 4: STILL NEED TO UPDATE VALUE OF C7428!</div> <div>2009-12-08: 1.3.0 csa 45: Added passive deemphasis to SATA HDD D2R lines: Added R4585, R4586 (51.1 ohm, 1% (11450093) and OMITTED Added R4585, C4586 (10pF, 5%, 13150029) and NOSTUFFED Added BOM table to stuff 0-ohms until we get go-ahead for filter</div> <div>2009-12-08: 1.4.0 csa 8: Deleted net properties for the following nets: =PP3V3_S0_CPUVTT1SENSE =PP5V_S0_HDP =PP5V_S0_MCPWRG0 =PP1V05_S0_MCP_AVDD_UF =PP3V3_S0_MCM_R =PP3V3_S0_PMRCTL =PP3V3_S0_DCCONN csa 34: Deleted net properties for =PP3V3_S3_WLAN csa 74: Changed C7434 from NOSTUFF to IMVP6:2PHASE per Intersil Added IMVP6:2PHASE to R7413 per Intersil Changed C7428 from 0.47uF to 0.33uF (132S0101) per Intersil Changed component color to green Cosmetic Cleanup csa 90: Deleted net properties for =PP5V_S3_CAMERA csa 98: Deleted net properties for =PPBUS_S0_LCDCLKLT csa 108: Added NET_PHYSICAL property to SATA_HDD_D2R_FILT_P and _N</div> <div>2009-12-09: 1.5.0 multiple: Added parentheses for SYNC_DATE property on all pages that have broken sync. csa 4: Deleted entry in Module Parts table for R6612, R6617, R6630, R6633 since they were removed when we switched from piezo to dynamic speakers csa 69: Changed J6955 symbol to K87 Hall effect assembly (339S0114)</div> <div>2009-12-10: 1.6.0 csa 69: Added OMIT to J6955, BOM table to stuff K84 Hall effect connector</div> <div>2009-12-11: 1.7.0 csa 45: Added PLACEMENT NOTE for passive deemphasis circuit. csa 74: Changed 1PHASE BOM table to correctly call out 132S0080 (0.22uF) instead of 0.022uF</div> <div>2009-12-16: 1.8.0 *** Resynced all synced pages and picked up the following (change notes from T27): csa 18: T27: Swapped USB_EXTB and USB_EXTD for NVRN-612340 (pg. 18). <radar:7416825> Ensure USB_EXTB is on ports 8-11 (NVRN-612340) csa 20: T27: Changed USB_RBIAS from 931-ohms to 887-ohms per DG v1.3 (pg. 18). <radar:7459260 > Design Guide v1.3 updates *** Started syncing the following pages: csa 29,31: T27: Added CKPLUS_WALVE properties to dismiss false errors (pg. 201). <radar:7368529> TASK: Waive false CheckPlus errors csa 54: T27: Added BOMPTIONS and APNs for Foxconn and Molex 80-DIMM connectors (pg. 29, 31). C5490 changed from CAP 402-0.022UF,10%,16V,CERM-XSR to CAP 402-0.022UF,20%,16V,CERM T27: Added CKPLUS_WALVE properties to dismiss false errors (pg. 54). T27: Added gain note for U5402 and SMC_BATT_SENSE (pg. 54). csa 57: T27: Changed RC balance on BATT_SENSE, same time constant (pg. 54). Began syncing from T27 per <radar:7304029 > T27 schematic bom option for R5714 & R5030 to keep K87 in sync R5714 has BOMPTION LED:K6_K69, and we need to substitute a different part on csa 4 *** Made the following changes to follow T27 on the following unsynced pages: csa 25: T27: Removed R2575 & R2580 per DG v1.3 (pg. 25). per <radar:7459260 > Design Guide v1.3 updates *** Other changes: csa 4: Added BOM table to substitute in parts that have BOMPTION xxxx:K6_K69 (to allow sync with T27) Added R5714 (11450125) to table with BOMPTION LED:K86_K87</div> <div>2009-12-17: 1.9.0 csa 4: Added BOM table entry for MCP89-A02 per <radar:7416858 > Task: Get part numbers for A02 rev. csa 34: Changed K87_MCP BOM group to call out MCP89-A02 Changed R3440 from A02 part to AP016 (343S0511) per <radar:7459498> BOM: APN updates for PFP1009 and SAK parts Changed R3454 to 100K, 1% (11450411) to match T27 and K69 Updated DLY text note for U3440 to match T27 Changed R3440 color to green, deleted WF text note about needing PU csa 72: Changed R3420 from 15250691 to 15250778 per <radar://problem/7347216> K69 L7260 combo footprint Alternates table on csa 4 already has 15250778 as alternate to 15250693</div> <div>2009-12-22: 1.10.0 csa 4: Per <radar://problem/7473229> K86: Move to MCP83 Added BOM table entry for MCP83M (337S3876) This is for K86 ONLY. Adding entry to minimize delta on csa 4 between K87 and K86 BOMPTION is MCP83M Per <radar://problem/7495072> K87: Call out LED:K86_K87 BOMPTION in the K87_MISC BOM group Added LDO:K86_K87 BOMPTION to the K87_MISC BOM group Per <radar://problem/7495116> K87: remove ON Semi alternate for Q2300 (376S0624) Removed table entry that says 376S0624 is an alternate for 376S0624 Per <radar://problem/7495021> K86/K87: Replace "S" APNs with "T" APNs for programmed SMC and BR Changed BOMPTION:K86 to call out LDO:K86_K87 BOMPTION (376S0624) Created SMC:PROG_K87 pointing to 34170252 (SUBASSY, IC, SMC, K87) Created SMC:PROG_K86 pointing to 34170250 (SUBASSY, IC, SMC, K86) Changed K87_PROGPARTS BOM group to point to SMC:PROG_K87 csa 69: Per <radar://problem/7494087> K87: remove OMIT from J6955 and delete BOM table Deleted BOM table for Hall effect assembly Changed text note to say "HALL EFFECT ASSEMBLY" Deleted OMIT BOMPTION from J6955 Added text note with part numbers for components of the assembly Assembly APN: 3350114 - BOM: 639-0680 - PCB: 056-2801 - MCO: 056-3515 Conn APN:51850788 csa 74: Cosmetic change, moved R7413, C7406 BOMPTION label so they don't look like wire name csa 78: Per <radar://problem/7495000> K87: Add NOSTUFF to R872 to disconnect U8790 from ALL_SYS_PWRGD Changed BOMPTION for R872 from SUPGOOD_ISL to NOSTUFF</div> <div>2010-01-06: 1.11.0 csa 7: Per <radar://problem/7517432> K86/K87 functional net property needed on signals in schematics Added the following functional test points under the J5100 LPC/SP1 CORN FUNC_TEST group LPCPLUS_GP10 LPC_SERIRQ SMC_TMS</div> <div>2010-01-07: 1.12.0 csa 23: *** BROKE SYNC WITH T27 Per <radar://problem/7519025> K86/K87: update all instances of 376S0786 schematic symbols Updated Q2355 and Q2356 with new schematic symbols Need to resync with T27 once the change has been made there csa 70: Per <radar://problem/7519048> K86/K87: change U7000 to 353S2929 Changed U7000 from 353S2392 to 353S2929 Updated APN text note</div> <div>2010-01-08: 2.0.0 csa 45: Per <radar://problem/7524364> K86/K87: change SATA HDD D2R passive EQ values Removed NOSTUFF from C4585, C4586 Removed OMIT from R4585, R4586 Deleted BOM table that stuffed the bypass option Changed R4585, R4586 to 11450065 (27.4 ohm, 1%) Changed C4585, C4586 to 13154713 (47pF, 5%)</div> <div>2010-01-13: 2.1.0 csa 4: Per <radar://problem/7540383> K86: Update CPU part number to 337S3792 Changed U1000 CPU:1.2GHZ BOMPTION from 337S3779 to 337S3792</div> <div>2010-01-13: 2.2.0 csa 4: Cosmetic: changed text sizes and alignment Per <radar://problem/7540522> K86/K87: Production Debug Components Changed D85-1093 to call out K87_DEVEL_PVT instead of K87_DEVEL_ENG Changed K87_COMMON to call out K87_DEBUG_PVT instead of K87_DEBUG_ENG Diff from the two changes above: Toggled: VREFMRCN:YES ==> VREFMRCN:NO BMON:ENG ==> BMON:PROD BKLT:ENG ==> BKLT:PROD SENS_R:ENG ==> SENS_R:PROD Removed: DEBUG_ADC, SUPGOOD_ISL, EFI_DEBUG, MCPPLL_LDO, EXTIV05, MCP_T_DIODE_SENSOR, XDP_CON Unchanged: LPCPLUS_DEVEL_BOM, SMC_DEBUG:YES, XDP Added LPCPLUS_CON to K87_DEVEL_ENG (does not change BOM for DVT) Changed all instances of K87_DEBUG_XXXX to K87_DEBUG:XXXX Changed all instances of K87_DEVEL_XXXX to K87_DEVEL:XXXX csa 51: (Per <radar://problem/7540522> K86/K87: Production Debug Components) Changed J5100 BOMPTION from LPCPLUS to LPCPLUS_CON to unstuff connector at DVT</div> <div>2010-01-15: 2.3.0 csa 74: Per <radar://7525313 > K86 CPU loadline, OCP update Keeping K86 and K87 pos identical for CSA 74, modifying BOM table for IMVP 1 phase on K87's schematic to reflect changes for K86. IMVP6:1PHASE BOM Table: R7417 changed to 7.87K (APN 11450305) R7416 added to BOM Table, 16.9K (APN 11450336) Added IMVP6:2PHASE BOM option to R7416 for K87's 13.7K csa 74, csa 79: Per <radar://7542674 > K86/K87 Text note change Cleaned up text notes for lphase, 2phase, and edp #s per radar request.</div> <div>2010-01-18: 2.4.0 csa 4: Per <radar://problem/7549122> K86/K87: Switch to new BOM group structure Reverted back to ENG BOM, no longer PROD BOM (i.e. reverted much of 2.2.0 changes) Changed BOM group structure to match that in the radar (see PDF attached to radar) Net change was to move LPCPLUS to the 639 (from the 085) Switching from Engineering to Production BOM should only require changing PROJECT_PHASE:DEV to PROJECT_PHASE:PROD Per <radar://problem/7544629> K86/K87: Update MCP83 description on SMC:PROG_K87 Changed Description for 337S3876 to "IC,MCP83M-A02,31X31MM,BGAL168" *** Started syncing with K6 Syncing with K6 to pick up new symbols for Q2355 and Q2356 Should switch syncing back to T27 once it is updated there csa 37: Per <radar://problem/7548726> K86/K87 Ethernet series R's need to be 0 ohmed Changed R3790-R3795 to 116S0094 (0-ohm, 0402) from 22-ohm</div> <div>2010-01-19: 2.5.0 csa 37: Per <radar://problem/7554342> K86/K87: Change L3720 to 152S1182 Changed L3720 to 152S1182 (IND,PWR,SHD,4.70H,20V,0.91A,31X31X12MM) for lower ESR</div> <div>2010-01-22: 2.6.0 csa 41: Per <radar://problem/7571786> K86/K87: Add E3T EEE code for K86 to schematic Added row to EEE table for E3T Changed BOMPTIONS to be mutually exclusive (changed "_" to "::")</div> <div>2010-01-28: 2.7.0 *** Resynced with T27 and K6 (no differences) *** Resynced Audio pages with the following changes: csa 45: -pg. 62: changed R6211 to 22 Ohms -pg. 67: no stuffed R6712 and R6713 Per <radar://problem/7561001> K87 BOM: Radiated Emissions: Right Audio emissions fail Added L4530, L4531 (APN 155S0137) to S1L connector pins csa 97: Per <radar://problem/7589365> K86/K87: Compensation settings change to provide more phase margin, reduce ripple Changed R9725 from 22k to 10k (11450315) and removed NOSTUFF Changed C9705 from 8.2nF to 33nF (132S0131) Changed C9706 from 120pF to 220pF (131S2225)</div> <div>2010-02-02: 2.8.0 *** Resynced with T27 and K6 (no differences) *** Resynced Audio pages with the following changes: csa 97: -pg. 67: added BOM options for U6700, R6712, and R6713 to support MAX14560 and MAX14504 - Changed R9710 from 7.32K 0402 1% to 7.68K (APN 11450304) to support old K84 panel csa 41: Added OLD_AUDIO_SWITCH BOM OPTION to K86_K87_COMMON</div> <div>2010-02-15: 2.9.0 2010-02-15: 2.10.0 csa 54: Broke sync with T27. Per <radar://problem/7605797> K69/K86/K87 sensor IN1C unreliable U5400 changed from OPA348 to OPA330. C5434 changed to NOSTUFF</div> <div>2010-02-16: 2.11.0 Resync with T27 and K6. Clean up and rerelease schematic.</div> <div>2010-02-18: 2.12.0 Per <radar://7644836> K87 power component update csa 74: R7417 changed to 5.90K, C7428 changed to 0.47uF, C7434 changed to 0.033uF csa 75: R7572 changed to 147K to 10K (11450315) and removed NOSTUFF csa 70: R7015 changed to 56.2K, C7015 changed to 1000pF, C7042 changed to 0.068uF Per <radar://7634730> K86/K87: add an RC on the LVDS_IG_BKL_PWM csa 97: R9725 changed to 200ohm, C9799 of 47pF added. R9726.1 connection moved to LVDS_IG_BKLPWM</div> <div>2010-02-18: 2.16.0 Per <radar://7676934> K86/K87: Hall eff documentation change. Substitute 607-6831 for doc purposes csa 69: J6955 BOMPTION change to OMIT. Added BOM table with 607-6831 for J6955 Per <radar://7488543> K86/K86 Task: Measure each power supply in mLB csa 74: For K86 only: C1204 = 0.7uF added, R7417 changed to 8.25kohm csa 12: For K86 only: C1272 = 330uF added. Per <radar://7685202> K86/K87 schematic: change U9700 to 353S2965 for Freescale backlight issue csa 97: U9700 changed to APN 514-0718 to 514-0750</div> <div>2010-02-18: 2.17.0 Per <radar://7686179> K86/K87 schematic: Change audio jack part number for new connector cap csa 67: J6700 changed from APN 514-0718 to 514-0750</div> <div>2010-02-25: 2.18.0 Per <radar://7485811> K86/K87 schematic: add additional 639 for differentiation between Foxconn and Molex DIMM connectors csa 4: MOLEX_DDR_CONN added to Module Parts, removed from Alternate table. Added second 639 and EEEE to BOM table</div> <div>2010-02-25: 2.19.0, 2.20.0 Per <radar://7678513> K87:EMC:ESD: System hangs on air/contact discharge to MPM connector csa 69: C6970, C6971, C6972 of 1000pF (APN 131S0222) added</div> <div>2010-02-26: 2.21.0 Per <radar://7488543> K87/K86 Task Measure each power supply in mLB. csa 12: C1208, C1204, C1207, C1209, C1211, C1219, C1202, C1216 NOSTUFFED csa 12: Added pads for 0603 caps (APN 138S0635). Components C1230, C1231, C1232, C1233, C1234, C1235, C1236, C1237. csa 74: Changed C7434 from 0.033uF to 0.047uF (APN 132S0189) per Liang</div> <div>2010-03-04: B.0.0 Per <radar://7683852> K87 Protol: 5 of 6 systems failing graphics noise (Underwater) acoustic spec by up to 3.1dB csa 12: C1233, C1230, C1232, C1234 changed from NOSTUFF to STUFFED.</div> <div>*** MLB_LDO branch</div> <div>2010-03-09: 0.8.0 Summary of changes for MLB_LDO: csa 25: U2590 added, APN 353S2971. R2592 of 10K and C2592 of 1uF, C2593 of 1uF added. Nets MCP_PLL_LDO_EN and PP3V3_S0_LDO_R added.</div> <div>2010-03-22: A.1.0 csa 25: Copied from K6 Added C2599, R2597, R2596, U2593, Q2592, R2599, C2594, U2594, R2598, C2598 with BOMPTION HTOL_SENSE:YES Added R2594 and R2591 with LDO:ADJ BOMPTION Changed BOMPTION names from LDO:YES and LDO:NO to MCPHVDV:P2V5 and MCPHVDV:P3V3 Added BOM TABLE with LDO:FIXED, LDO:ADJ, and HTOL_SENSE:NO stuffing options csa 50: Removed SMC alias to TP for SMC_NB_MISC_SENSE to enable sense circuitry connection to SMC Removed SMC_P10 alias to TP SMC_P10 csa 81: Added =PP3V42_G3H_OPA330 alias to power U2594 Added =PP3V3_S0_OPA330 alias to power U2593 csa 4: Added MCPHVDV:P2V5, LDO:FIXED, HTOL_SENSE:YES to BOM Group K86_K87_DEBUG:PROD</div> <div>2010-03-22: A.2.0 Per <radar://7783507> K87: Add cap to DDC line to avoid DDC line glitch issue csa 93: Added C9303 3300pF cap on DP_CA_DET. csa 25: Changed U2594 power to 3V3_S0 from 3V42_G3H.</div> <div>2010-03-22: A.3.0 csa 77: Deleted U7740 1.05V LDO circuit to free space for U2592 and current mirror circuit.</div> <div>2010-03-22: A.4.0 Reverted the changes and synced back to A.0.0 Per <radar://7783507> K87: Add cap to DDC line to avoid DDC line glitch issue csa 93: Added C9303 3300pF cap on DP_CA_DET.</div> <div>2010-03-22: A.5.0 csa 25: Added R2591,R2594 for LDO:ADJ option. Changed U2592 to LDO:FIXED option. csa 4: Added Alternate part for U2592 LDO. 353S2987(TI), 353S2988(Micrel) to 353S2986(Intersil). LDO:FIXED, MCPHVDV:P2V5 added in bom table.</div> <div>2010-03-30: A.7.0 Reverted the changes and synced back to A.2.0 csa 4: Added Alternate part for U2592 LDO. 353S2987(TI), 353S2988(Micrel) to 353S2986(Intersil). LDO:FIXED, MCPHVDV:P2V5 added in bom table.</div> <div>2010-03-31: A.8.0 csa 25,49,50: Changed Q2592 gate control pin to SMC_P24 from SMC_P10.</div> <div>2010-04-1: A.9.0 csa 25: Added R2600 0ohm resistor to help layout change.</div> <div>2010-04-1: A.10.0 csa 25: Changed R2600 refiles to R2550 to match with page#.</div> <div>2010-04-14: B.0.0 rdar://7822714 csa 69: R6905 kept same lohm. C6900 changed to 2.2uF. 138S0592. csa 4: Devel BOM# changed to 085-1799. And BOM OPTIONS to K86_K87_DEVELOPMENT_PVT. Removed Intersil LDO(353S2986).</div> <div>2010-04-14: C.0.0 csa 4: Added Toshiba(376S0908), Fairchild(376S0907) as an alternate to 376S0634. Added Onsemi new spec part(376S0912) as an alternate to Q2300(376S0868).</div>							
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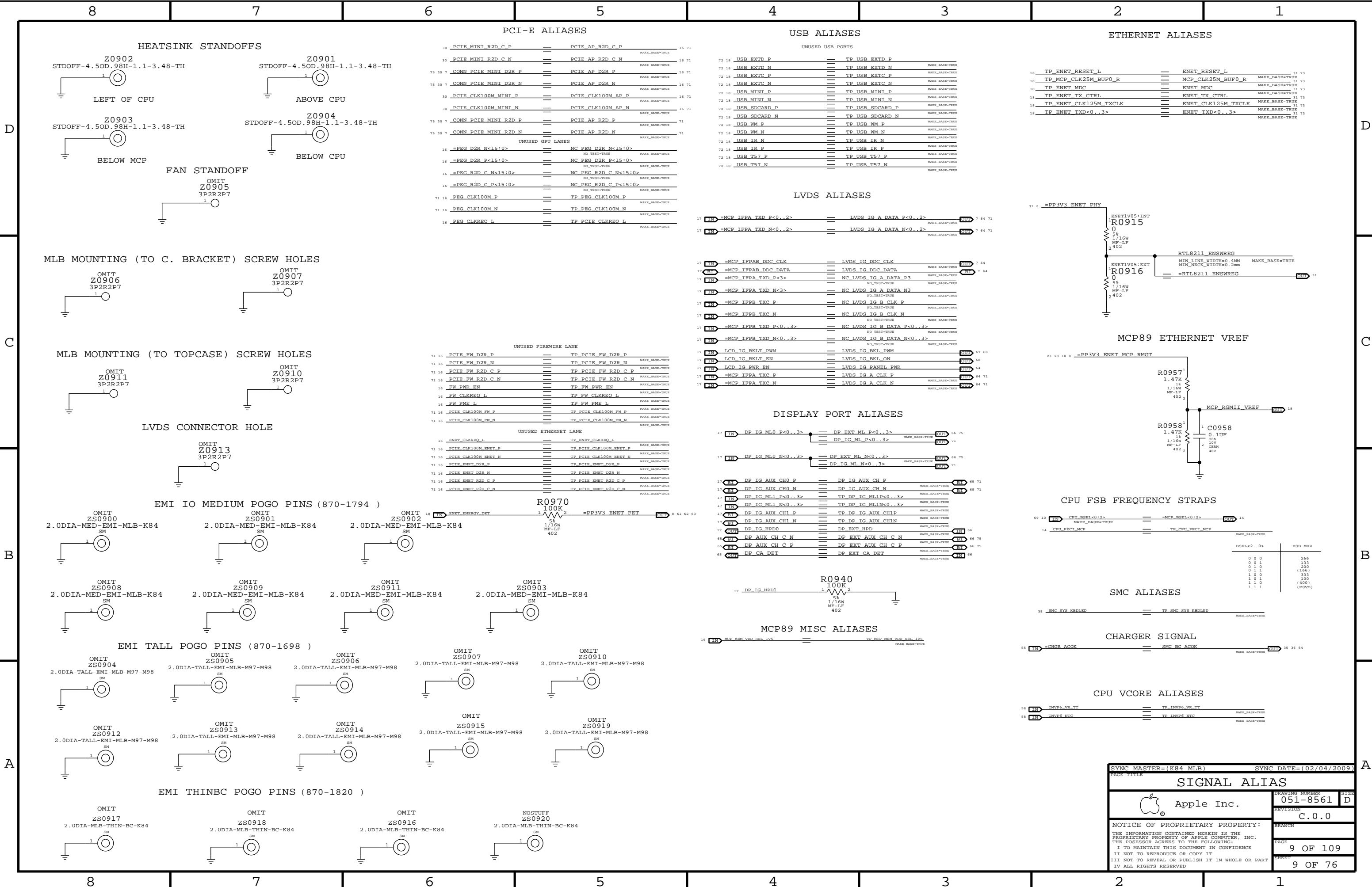
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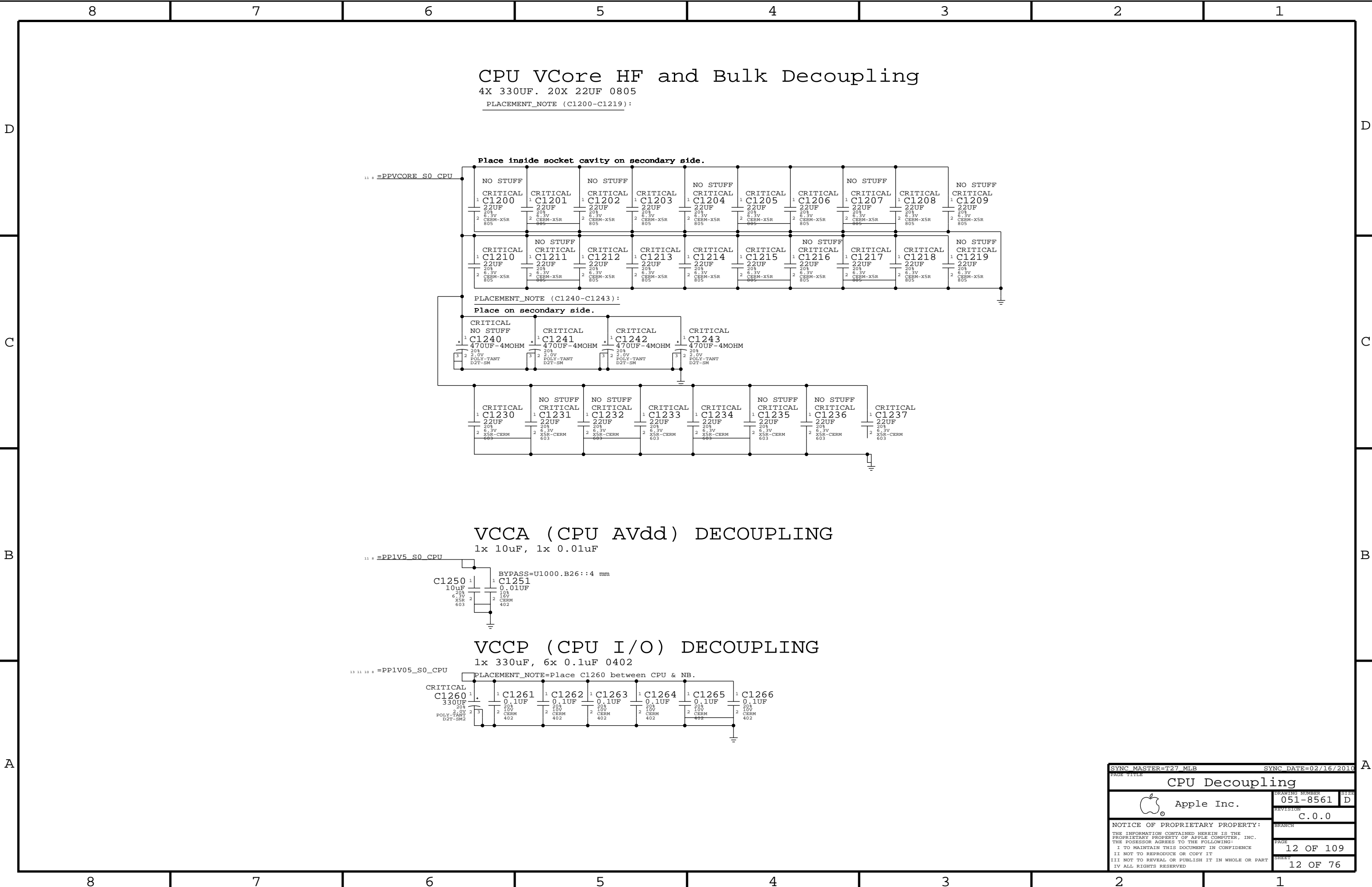
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Functional Test Points							
FAN CONNECTORS FUNC_TEST							
PP30	TRUE	PP5V_S0	7 8 62				
PP30	TRUE	FAN_RT_PWM	42				
PP30	TRUE	FAN_RT_TACH	42				
(NEED TO ADD 1 GND TP)							
MIC FUNC_TEST							
PP30	TRUE	BI_MIC_N	52 53 75				
PP30	TRUE	BI_MIC_P	52 53 75				
PP30	TRUE	BI_MIC_SHIELD	52 53				
SPEAKER FUNC_TEST							
PP30	TRUE	SPKRAMP_L_N_OUT	51 52				
PP30	TRUE	SPKRAMP_L_P_OUT	51 52				
PP30	TRUE	SPKRAMP_R_N_OUT	51 52				
PP30	TRUE	SPKRAMP_R_P_OUT	51 52				
PP30	TRUE	SPKRAMP_SUB_N_OUT	51 52				
PP30	TRUE	SPKRAMP_SUB_P_OUT	51 52				
LVDS FUNC_TEST							
PP30	TRUE	PP3V3_S0_LCD_DDC_F	64				
PP30	TRUE	PP3V3_SW_LCD_PANEL_F	64 (NEED 2 TP)				
PP30	TRUE	PPVOUT_S0_LCDBKLT	7 46 64 67 (NEED 2 TP)				
PP30	TRUE	LVDS_IG_DDC_CLK	9 64				
PP30	TRUE	LVDS_IG_DDC_DATA	9 64				
PP30	TRUE	LVDS_IG_A_DATA_N<0>	9 64 71				
PP30	TRUE	LVDS_IG_A_DATA_P<0>	9 64 71				
PP30	TRUE	LVDS_IG_A_DATA_N<1>	9 64 71				
PP30	TRUE	LVDS_IG_A_DATA_P<1>	9 64 71				
PP30	TRUE	LVDS_IG_A_DATA_N<2>	9 64 71				
PP30	TRUE	LVDS_IG_A_DATA_P<2>	9 64 71				
PP30	TRUE	LVDS_IG_A_CLK_F_N	64 75				
PP30	TRUE	LVDS_IG_A_CLK_F_P	64 75				
PP30	TRUE	LED_RETURN_1	64 67				
PP30	TRUE	LED_RETURN_2	64 67				
PP30	TRUE	LED_RETURN_3	64 67				
PP30	TRUE	LED_RETURN_4	64 67				
PP30	TRUE	LED_RETURN_5	64 67				
PP30	TRUE	LED_RETURN_6	64 67				
PP30	TRUE	PP5V_S3_CAMERA_F	7 64				
PP30	TRUE	USB_CAMERA_CONN_P	64 75				
PP30	TRUE	USB_CAMERA_CONN_N	64 75				
(NEED TO ADD 5 GND TP)							
SATA ODD CONN FUNC_TEST							
PP30	TRUE	PP5V_SW_ODD	7 33 46 (NEED 4 TP)				
PP30	TRUE	SMC_ODD_DETECT	33 35				
PP30	TRUE	SATA_ODD_D2R_C_P	33 71				
PP30	TRUE	SATA_ODD_D2R_C_N	33 71				
PP30	TRUE	SATA_ODD_R2D_P	33 71				
PP30	TRUE	SATA_ODD_R2D_N	33 71				
(NEED TO ADD 4 GND TP)							
SATA HDD/SIL FUNC_TEST							
PP30	TRUE	PP5V_S0_HDD_FLT	7 33 (NEED 4 TP)				
PP30	TRUE	SATA_HDD_R2D_P	33 71				
PP30	TRUE	SATA_HDD_R2D_N	33 71				
PP30	TRUE	SATA_HDD_D2R_C_P	33 71				
PP30	TRUE	SATA_HDD_D2R_C_N	33 71				
PP30	TRUE	SYS_LED_ANODE_R	33				
(NEED TO ADD 4 GND TP)							
BATT POWER CONN FUNC_TEST							
PP30	TRUE	PPVBAT_G3H_CONN	54 55 (NEED 3 TP)				
PP30	TRUE	SMBUS_SMC_BSA_SCL	38 74				
PP30	TRUE	SMBUS_SMC_BSA_SDA	38 74				
PP30	TRUE	SYS_DETECT_L	54				
(NEED TO ADD 3 GND TP)							
HALL EFFECT CONNECTOR FUNC_TEST							
PP30	TRUE	PP3V42_G3H	7 8 (NEED 2 TP)				
PP30	TRUE	SMC_LID_R	54				
(NEED TO ADD 3 GND TP)							
X16 WIRELESS CONN FUNC_TEST							
PP30	TRUE	PP3V3_S3_BT_F	30				
PP30	TRUE	CONN_PCIE_MINI_D2R_P	9 30 75				
PP30	TRUE	CONN_PCIE_MINI_D2R_N	9 30 75				
PP30	TRUE	CONN_PCIE_MINI_R2D_P	9 30 75				
PP30	TRUE	CONN_PCIE_MINI_R2D_N	9 30 75				
PP30	TRUE	PCIE_CLK100M_MINI_CONN_P	30 75				
PP30	TRUE	PCIE_CLK100M_MINI_CONN_N	30 75				
PP30	TRUE	PP3V3_WLAN (NEED 4 TP)	7 30				
PP30	TRUE	PCIE_WAKE_L	16 30				
PP30	TRUE	CONN_USB2_BT_P	30 75				
PP30	TRUE	CONN_USB2_BT_N	30 75				
PP30	TRUE	AP_CLKREQ_O_L	30				
PP30	TRUE	AP_RESET_CONN_L	30				
(NEED TO ADD 4 GND TP)							
IPD_FLEX_CONN FUNC_TEST							
PP30	TRUE	PP3V3_S3	7 8				
PP30	TRUE	PP18V5_S3	7 44				
PP30	TRUE	Z2_CS_L	43 44				
PP30	TRUE	Z2_DEBUG3	43 44				
PP30	TRUE	Z2_MOSI	43 44				
PP30	TRUE	Z2_MISO	43 44				
PP30	TRUE	Z2_SCLK	43 44				
PP30	TRUE	Z2_BOOST_EN	44				
PP30	TRUE	Z2_HOST_INTN	43 44				
PP30	TRUE	Z2_CLKIN	43 44				
PP30	TRUE	Z2_KEY_ACT_L	43 44				
PP30	TRUE	Z2_RESET	43 44				
PP30	TRUE	PSOC_MISO	43 44				
PP30	TRUE	PSOC_MOSI	43 44				
PP30	TRUE	PSOC_SCLK	43 44				
PP30	TRUE	SMBUS_SMC_A_S3_SDA	38 74				
PP30	TRUE	SMBUS_SMC_A_S3_SCL	38 74				
PP30	TRUE	PSOC_F_CS_L	43 44				
PP30	TRUE	PICKB_L	43 44				
(NEED TO ADD 2 GND TP)							
KEYBOARD CONN FUNC_TEST							
PP30	TRUE	PP3V3_S3	7 8				
PP30	TRUE	PP3V42_G3H	7 8				
PP30	TRUE	WS_KBD1	43				
PP30	TRUE	WS_KBD2	43				
PP30	TRUE	WS_KBD3	43				
PP30	TRUE	WS_KBD4	43				
PP30	TRUE	WS_KBD5	43				
PP30	TRUE	WS_KBD6	43				
PP30	TRUE	WS_KBD7	43				
PP30	TRUE	WS_KBD8	43				
PP30	TRUE	WS_KBD9	43				
PP30	TRUE	WS_KBD10	43				
PP30	TRUE	WS_KBD11	43				
PP30	TRUE	WS_KBD12	43				
PP30	TRUE	WS_KBD13	43				
PP30	TRUE	WS_KBD14	43				
PP30	TRUE	WS_KBD15_CAP	43				
PP30	TRUE	WS_KBD16_NUM	43				
PP30	TRUE	WS_KBD17	43				
PP30	TRUE	WS_KBD18	43				
PP30	TRUE	WS_KBD19	43				
PP30	TRUE	WS_KBD20	43				
PP30	TRUE	WS_KBD21	43				
PP30	TRUE	WS_KBD22	43				
PP30	TRUE	WS_KBD23	43				
PP30	TRUE	WS_KBD_ONOFF_L	43				
PP30	TRUE	WS_LEFT_SHIFT_KBD	43				
PP30	TRUE	WS_LEFT_OPTION_KBD	43				
PP30	TRUE	WS_CONTROL_KBD	43				
(NEED TO ADD 1 GND TP)							
DC POWER CONN FUNC_TEST							
PP30	TRUE	PP18V5_DCIN_FUSE (NEED 2 TP)	54				
PP30	TRUE	ADAPTER_SENSE	54				
(NEED TO ADD 2 GND TP)							
POWER NETS FUNC_TEST							
PP30	TRUE	PPVCORE_S0_CPU	8 39				
PP30	TRUE	PPVCORE_S0_MCP	8 39				
PP30	TRUE	PP1V05_S0	8 62				
PP30	TRUE	PP1V5_S0	8 62 75				
PP30	TRUE	PP1V8_S0	8				
PP30	TRUE	PP5V_S0	7 8 62				
PP30	TRUE	PP5V_S0	7 8 62				
PP30	TRUE	PP3V3_S0	8 62 75				
PP30	TRUE	PP1V5R1V35_S3	8 75				
PP30	TRUE	PP3V3_S3	7 8				
PP30	TRUE	PP5V_S3	8				
PP30	TRUE	PP3V3_S5	8 62 75				
PP30	TRUE	PP3V42_G3H	7 8				
PP30	TRUE	PPBUS_G3H	8 39				
PP30	TRUE	PP0V9_ENET	8				
PP30	TRUE	PP3V3_ENET	8				
PP30	TRUE	PP3V3_G3_RTC	8 19 20 23				
PP30	TRUE	PP3V3_WLAN	7 30				
PP30	TRUE	PP5V_SW_ODD	7 33 46				
PP30	TRUE	PP5V_S0_HDD_FLT	7 33				
PP30	TRUE	PP3V3_S5_AVREF_SMC	35 36				
PP30	TRUE	PP18V5_S3	7 44				
PP30	TRUE	PP3V3_SW_LCD_PANEL_F	7 64				
PP30	TRUE	PPVOUT_S0_LCDBKLT	7 46 64 67				
PP30	TRUE	PP4V5_AUDIO_ANALOG	48				
PP30	TRUE	SMC_PM_G2_EN	35 62				
PP30	TRUE	PM_SLP_S4_L	19 35 36 62				
PP30	TRUE	PM_SLP_S3_L	19 35 62 66				
PP30	TRUE	PP5V_S3_CAMERA_F	7 64				
PP30	TRUE	PP0V9_S5	8				
PP30	TRUE	PPDDRVTT_S0	8				
PP30	TRUE	PP1V05_S0_MCP_PLL_UP	8				
PP30	TRUE	PPVTT_S3_DDR_BUF	8				
(NEED TO ADD 6 GND TP)							
FSB SIGNALS WITH NOTEST							
PP30	NO TEST	TRUE FSB_A_L<35..3>	10 14 69				
PP30	NO TEST	TRUE FSB_ADS_L	10 14 69				
PP30	NO TEST	TRUE FSB_ADSTB_L<1..0>	10 14 69				
PP30	NO TEST	TRUE FSB_D_L<63..0>	10 14 69				
PP30	NO TEST	TRUE FSB_DINV_L<3..0>	10 14 69				
PP30	NO TEST	TRUE FSB_DSTB_L_N<3..0>	10 14 69				
PP30	NO TEST	TRUE FSB_DSTB_L_P<3..0>	10 14 69				
PP30	NO TEST	TRUE FSB_HIT_L	10 14 69				
PP30	NO TEST	TRUE FSB_HITM_L	10 14 69				
PP30	NO TEST	TRUE FSB_LOCK_L	10 14 69				
PP30	NO TEST	TRUE FSB_REQ_L<4..0>	10 14 69				
J5100 LPC+SPI CONN FUNC_TEST							
PP30	TRUE	PP3V42_G3H	7 8				
PP30	TRUE	SPI_CLK	37 72				
PP30	TRUE	SPI_CS0_L	37 72				
PP30	TRUE	SPI_MISO	19 37 72				
PP30	TRUE	SPI_MOSI	37 72				
PP30	TRUE	SPIFROM_USE_MLB	19 37 47				
PP30	TRUE	LPCPLUS_GPIO	19 35 37				
PP30	TRUE	LPC_SERIRQ	19 35 37				
PP30	TRUE	SMC_TMS	35 36 37				
(NEED TO ADD 2 GND TP)							
FUNC TEST							
Apple Inc.							
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REVISION C.0.0							
PAGE 7 OF 109							
SHEET 7 OF 76							











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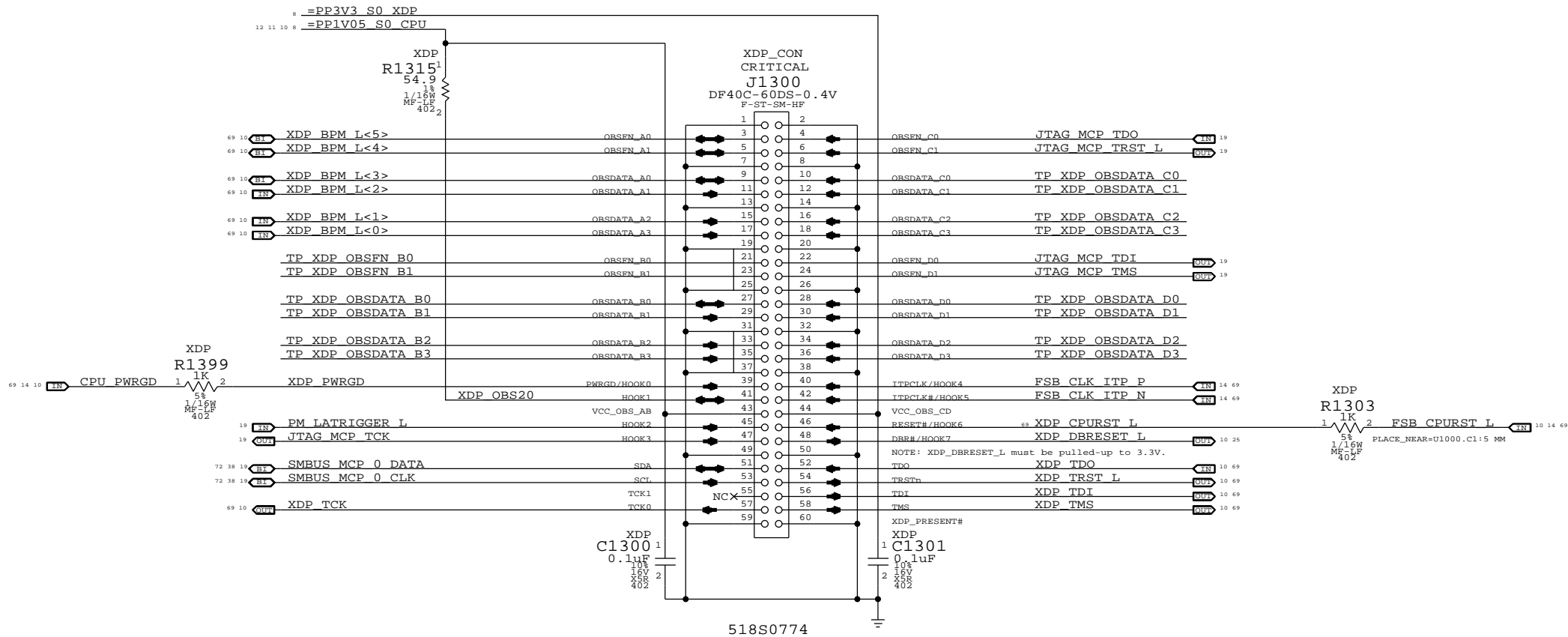
B

A


Mini-XDP Connector

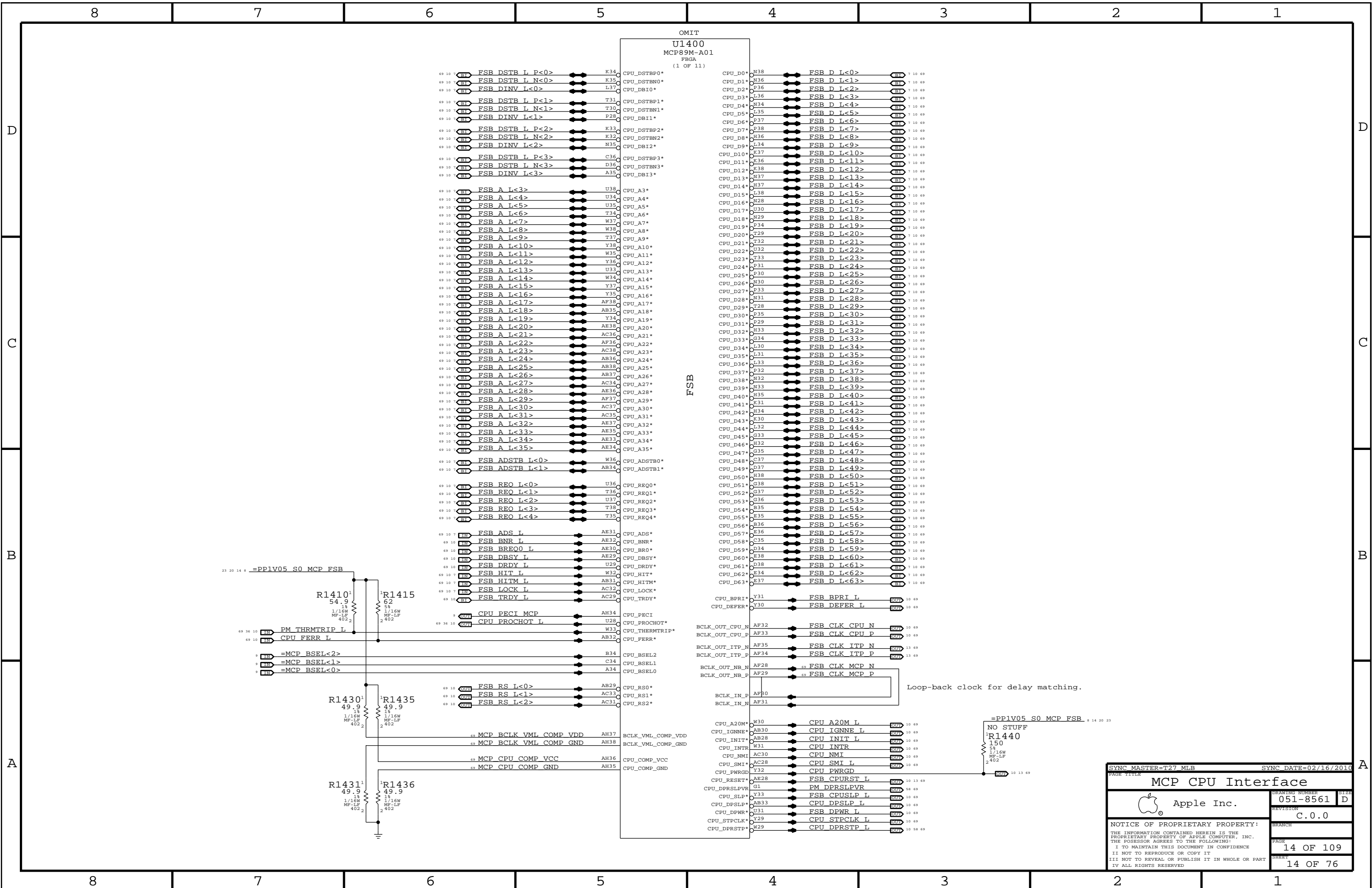
NOTE: This is not the standard XDP pinout.
USE WITH 920-0782 ADAPTER FLEX TO SUPPORT CPU, MCP DEBUGGING.

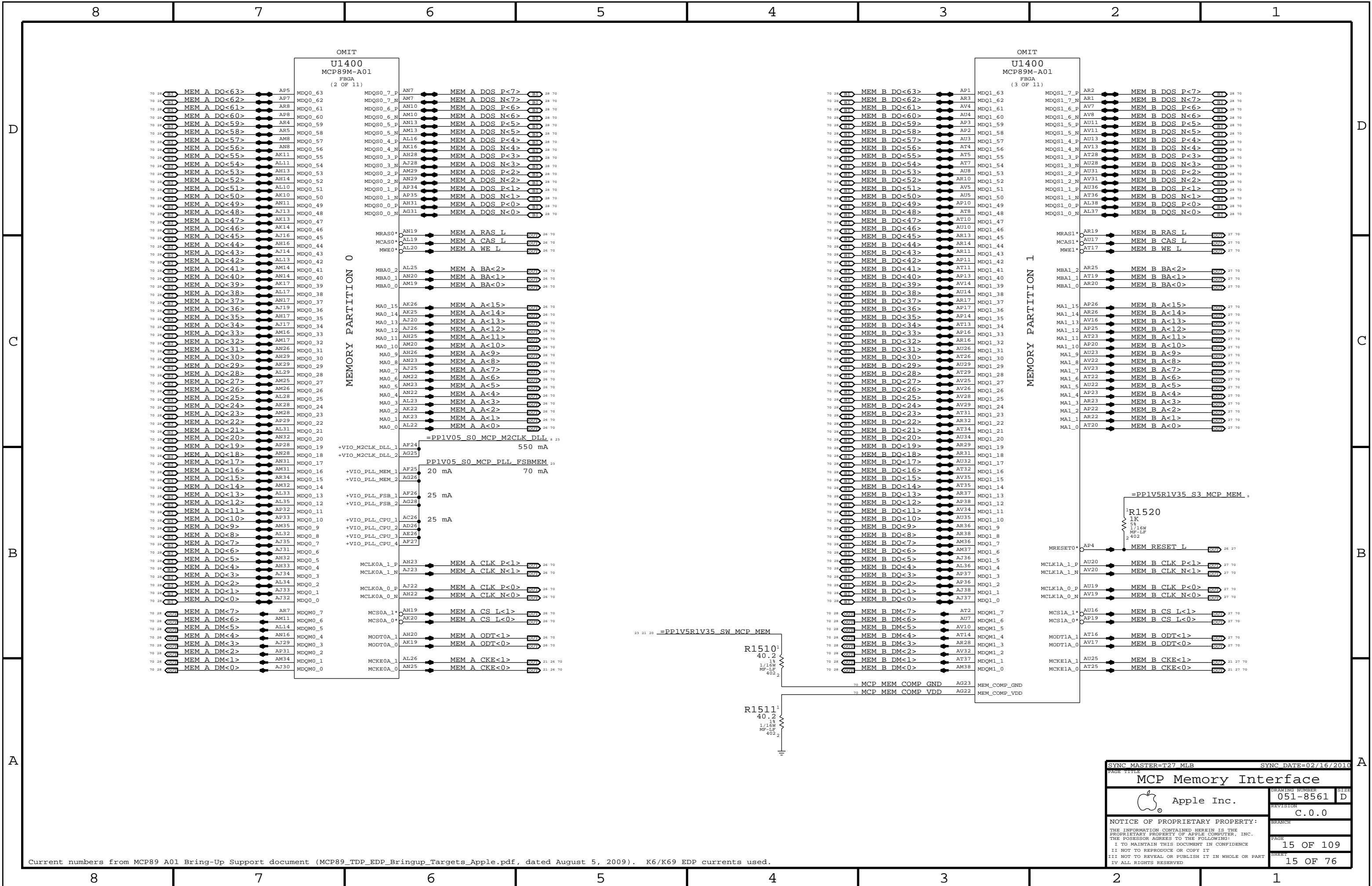
MCP89-SPECIFIC PINOUT



Direction of XDP module
Please avoid any obstructions
ON ODD-NUMBERED SIDE OF J1300

SYNC MASTER=(K84 MLB)		SYNC DATE=(02/25/2009)	
PAGE TITLE			
eXtended Debug Port (MiniXDP)			
		DRAWING NUMBER	051-8561
Apple Inc.		REVISION	C.0.0
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		PAGE	13 OF 109
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Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
MCP Memory Interface			
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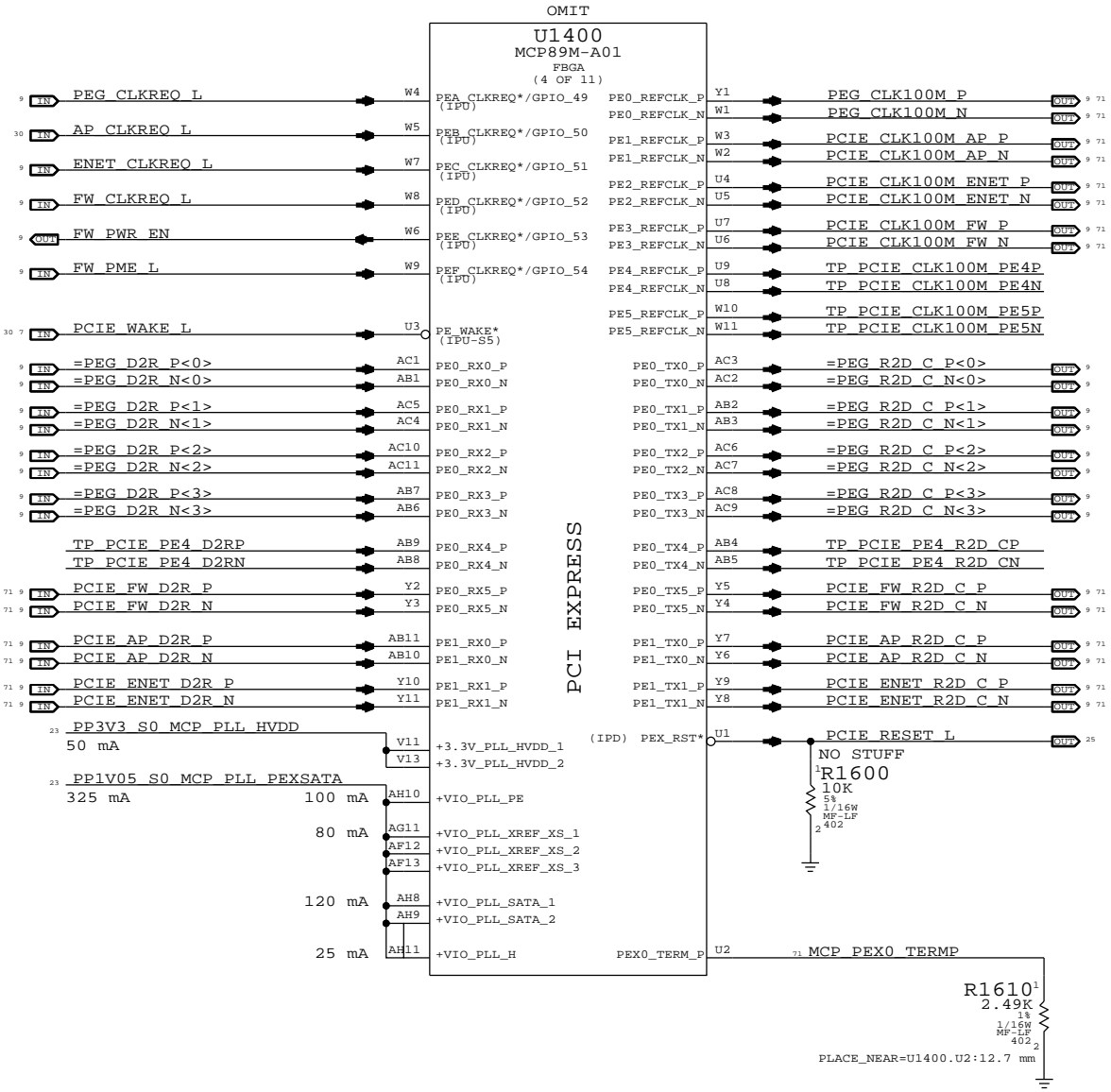
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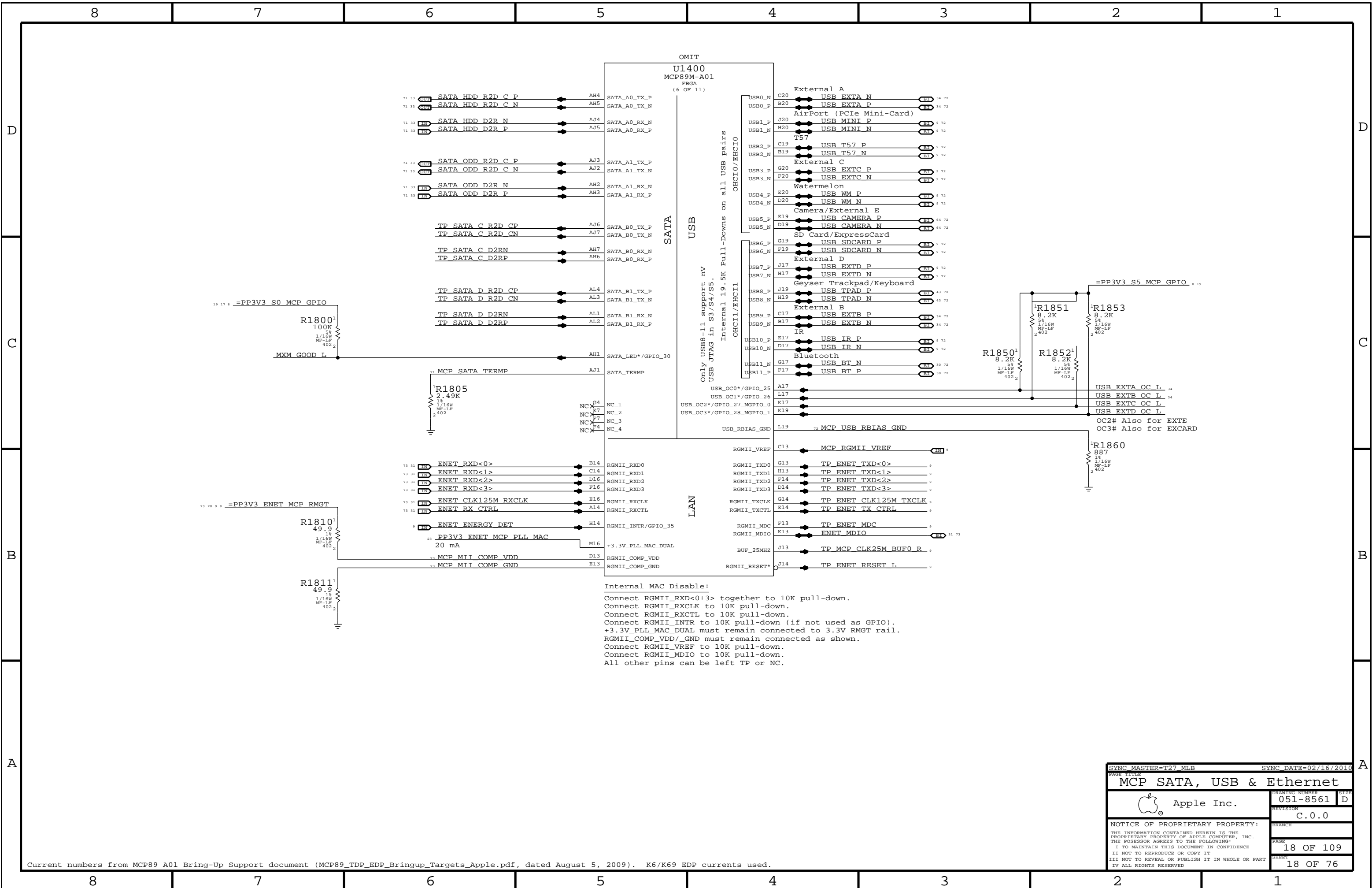
A




PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

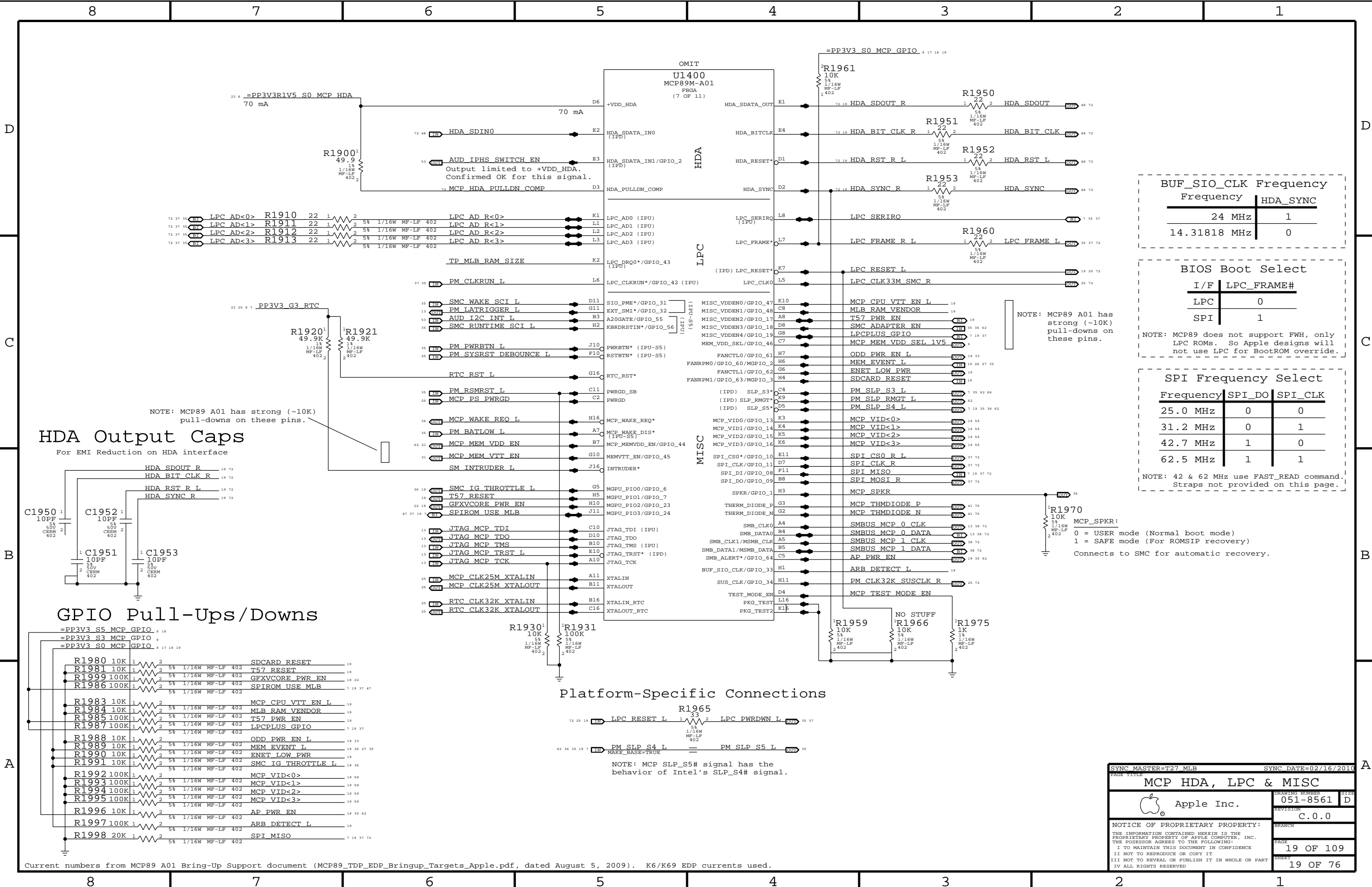
If PE0[3:0] are not used,
+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

If PE0[4:5] and PE1[0:1] are not used,
+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND



Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
MCP SATA, USB & Ethernet		DRAWING NUMBER	
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		REVISION	
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BUF_SIO_CLK Frequency	
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

BIOS Boot Select	
I/F	LPC_FRAME#
LPC	0
SPI	1

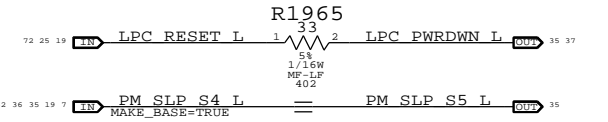
SPI Frequency Select		
Frequency	SPI_DO	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
42.7 MHz	1	0
62.5 MHz	1	1

NOTE: 42 & 62 Mhz use FAST_READ command. Straps not provided on this page.

NOTE: MCP89 A01 has strong (~10K) pull-downs on these pins.

MCP_SPKR:
0 = USER mode (Normal boot mode)
1 = SAFE mode (For ROMSIP recovery)
Connects to SMC for automatic recovery.

Platform-Specific Connections



NOTE: MCP SLP_S5# signal has the behavior of Intel's SLP_S4# signal.

SYNC MASTER=T27 MLB

SYNC DATE=02/16/2010

MCP HDA, LPC & MISC

Apple Inc.

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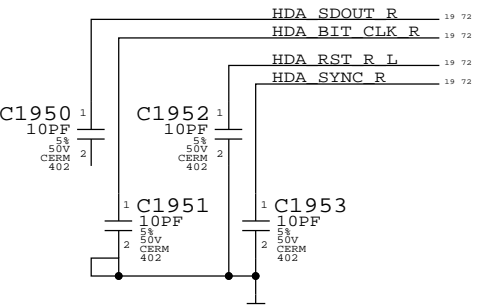
19 OF 109

SHEET

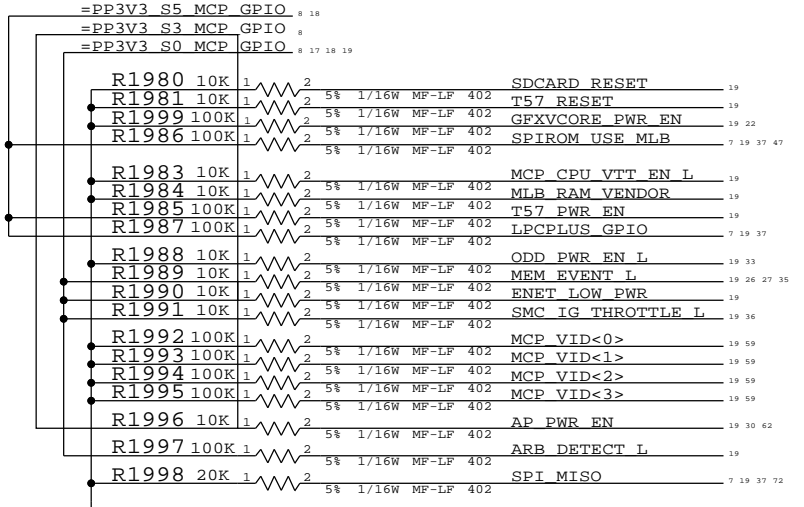
19 OF 76

HDA Output Caps

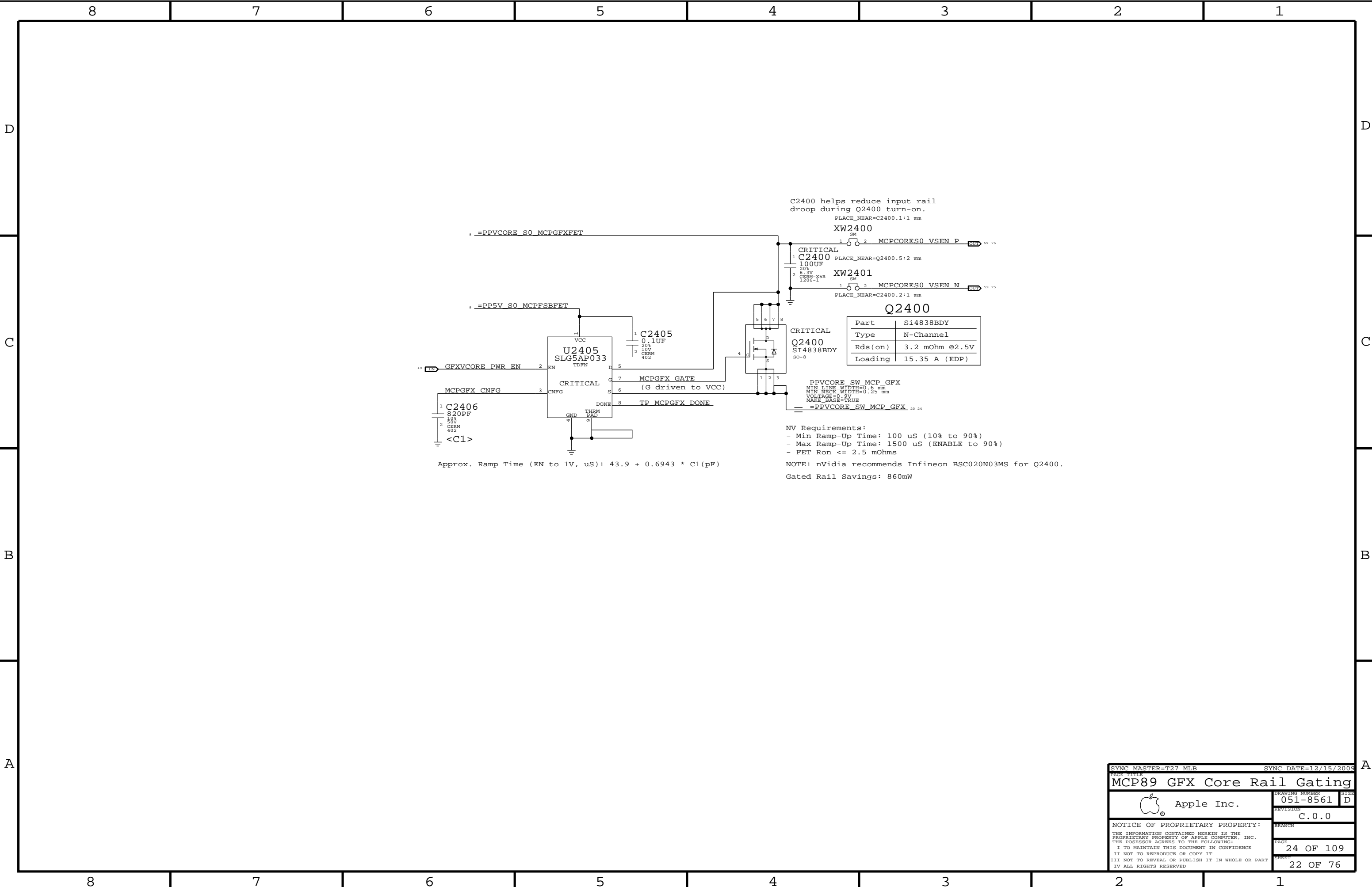
For EMI Reduction on HDA interface




GPIO Pull-Ups/Downs

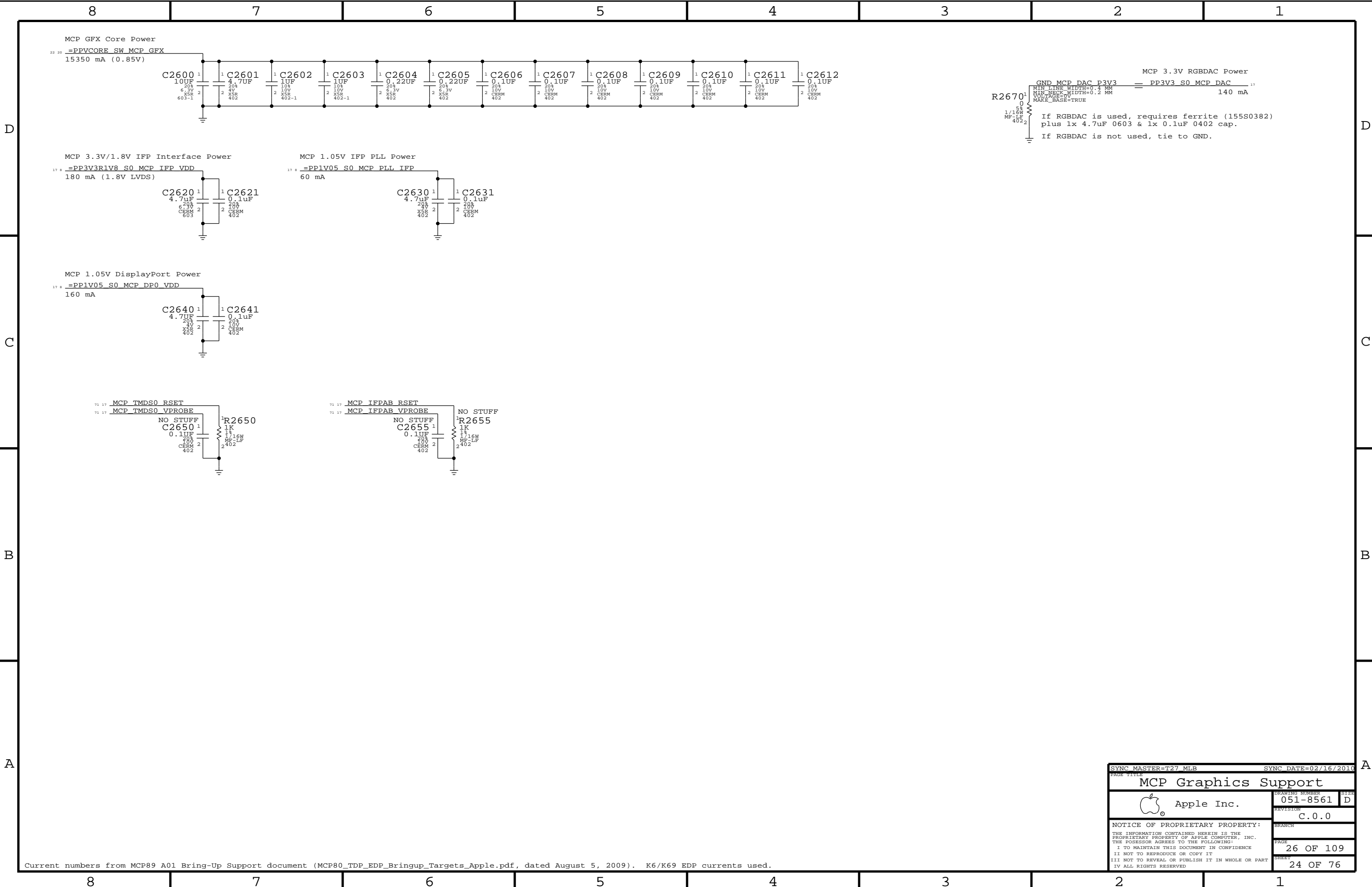


Current numbers from MCP89 A01 Bring-Up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.




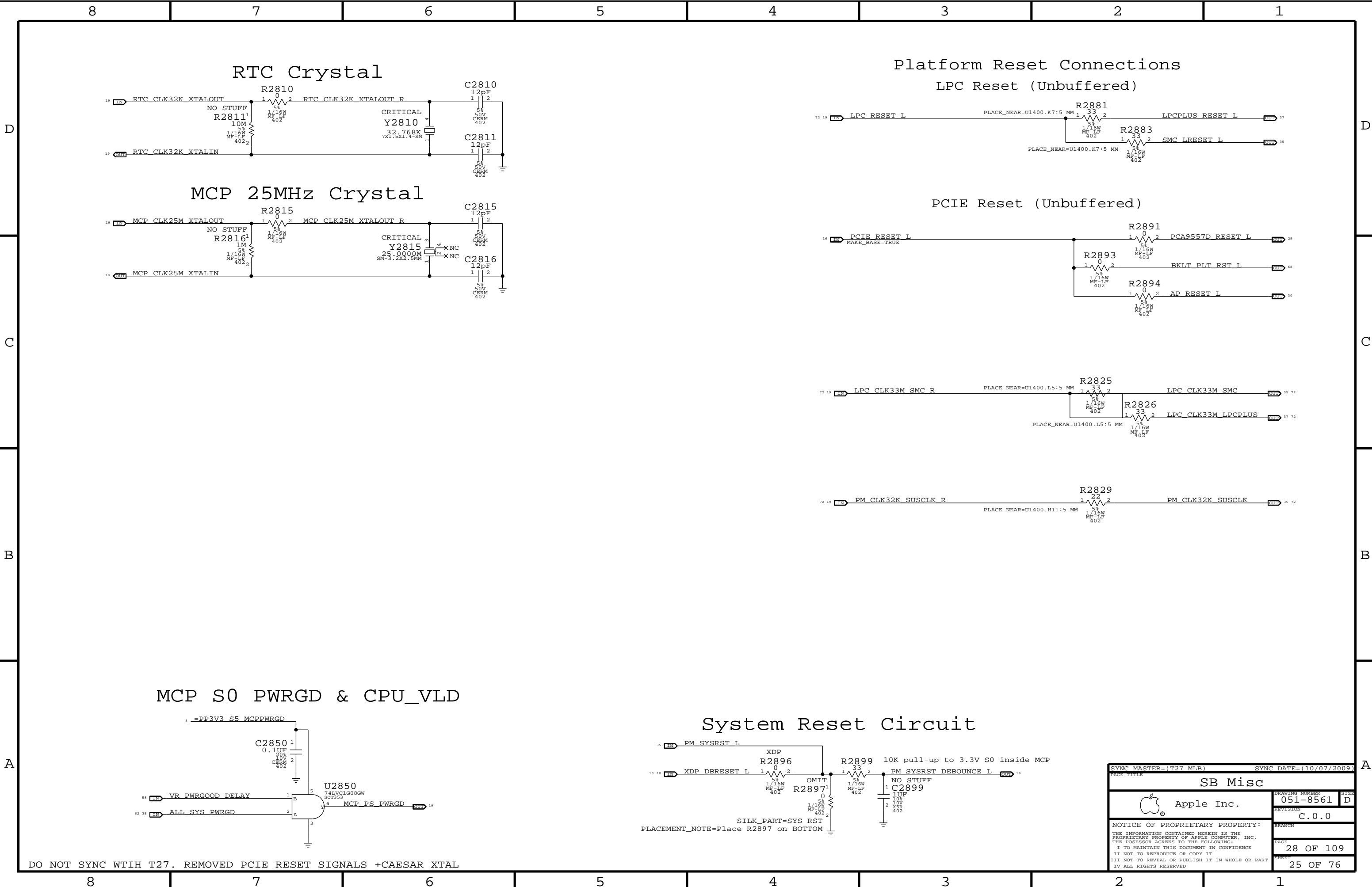


SYNCH MASTER=(T27 MLB)		SYNCH DATE=(11/16/2009)	
PAGE TITLE			
MCP Standard Decoupling			
 Apple Inc.		GRATING NUMBER	SIZE
		051-8561	D
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		25 OF 109	
SHEET			
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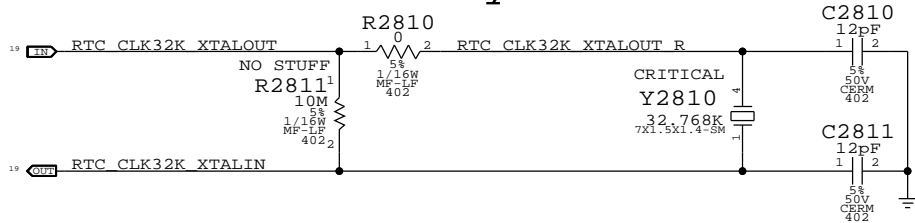


Current numbers from MCP89 A01 Bring-Up Support document (MCP80_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009). K6/K69 EDP currents used.

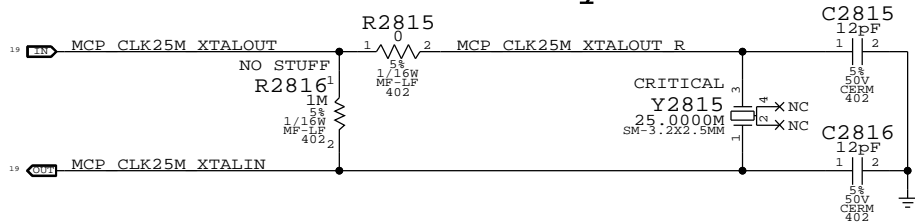
SYNC MASTER=T27_MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
MCP Graphics Support		Support	
 Apple Inc.		DRAWING NUMBER	051-8561
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RTC Crystal

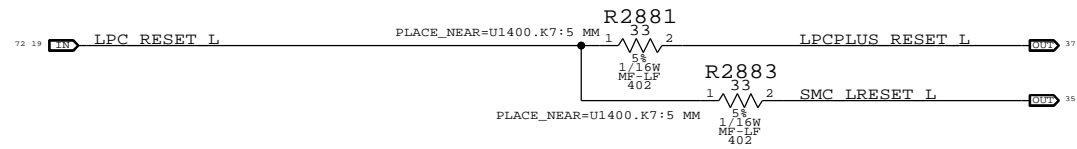


MCP 25MHz Crystal

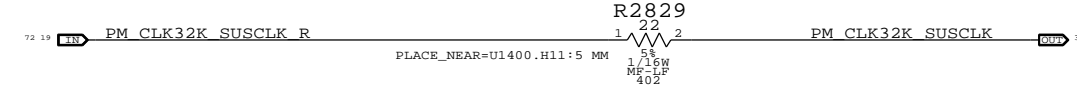
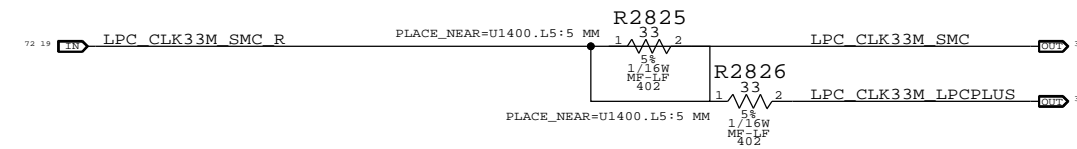
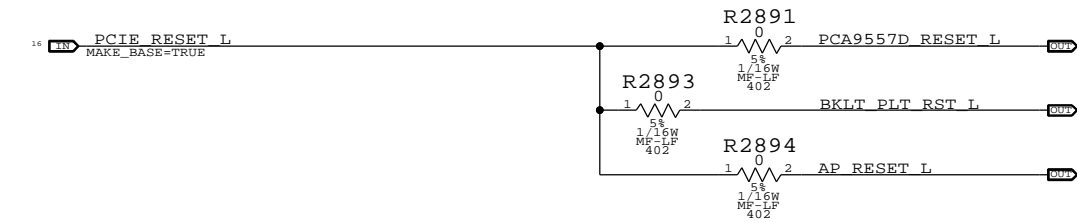


Platform Reset Connections

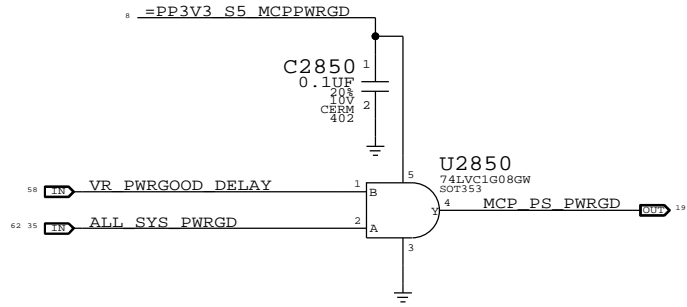
LPC Reset (Unbuffered)



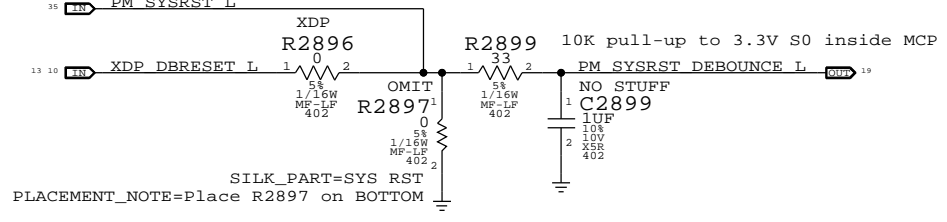
PCIE Reset (Unbuffered)



MCP S0 PWRGD & CPU_VLD



System Reset Circuit



PAGE TITLE		PAGE NUMBER	
SB Misc		051-8561	
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DO NOT SYNC WITH T27. REMOVED PCIE RESET SIGNALS +CAESAR XTAL

Page Notes

Power aliases required by this page:

- =PPLVDDR_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

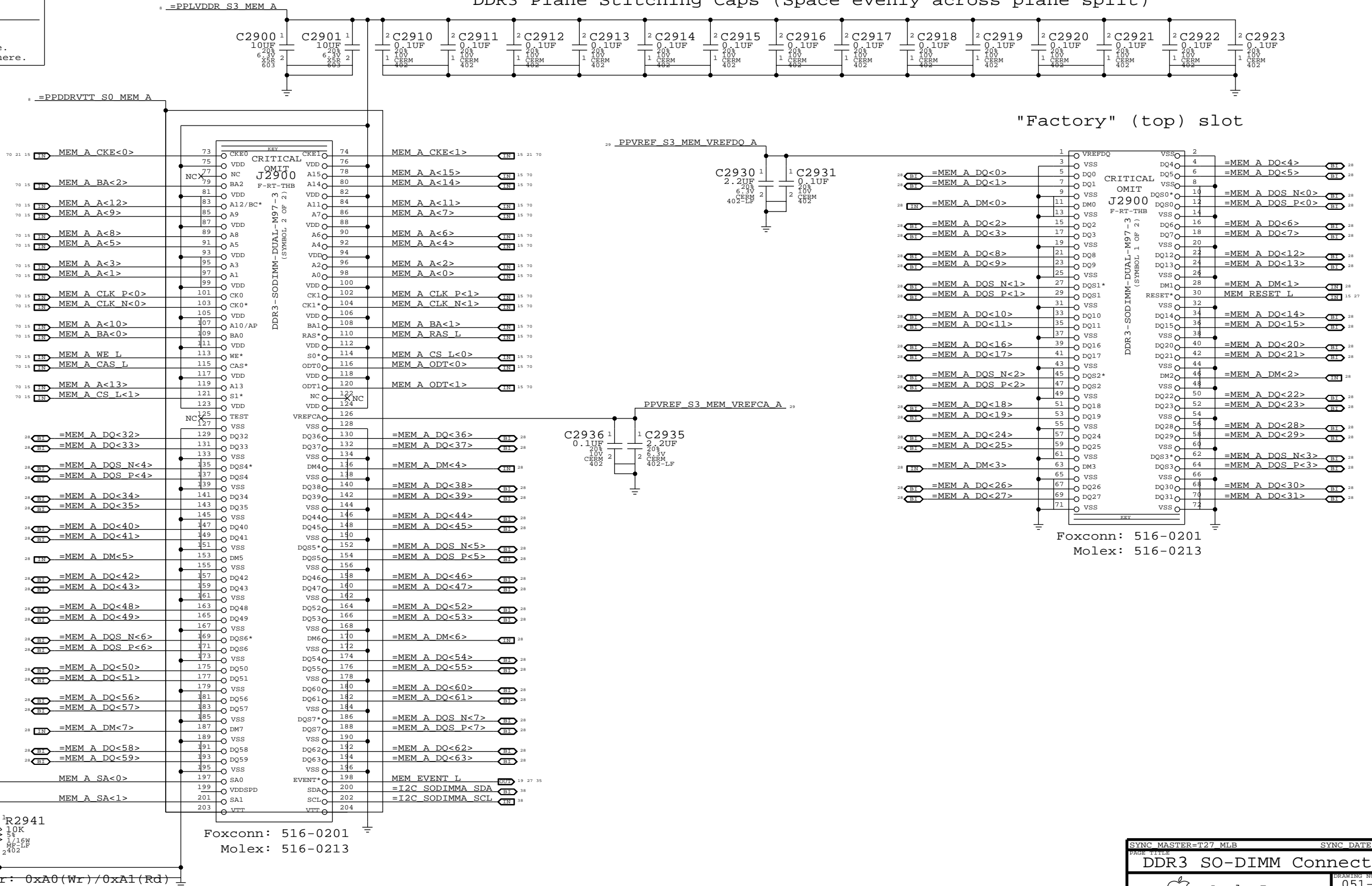
BOM options provided by this page:


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NOTE: J3100 is OMITted on this page.

Proper APN(s) required elsewhere.

DDR3 Plane Stitching Caps (Space evenly across plane split)



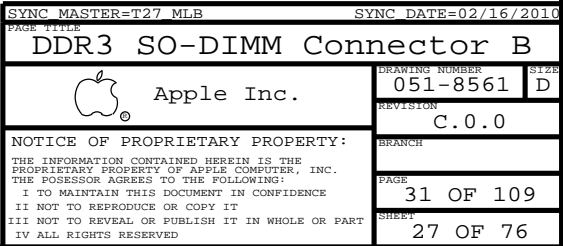
SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
DDR3 SO-DIMM Connector A			
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```
Power aliases required by this page:
- =PPLVDDR_S3_MEM_B
- =PPDDRVTTS_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)
```

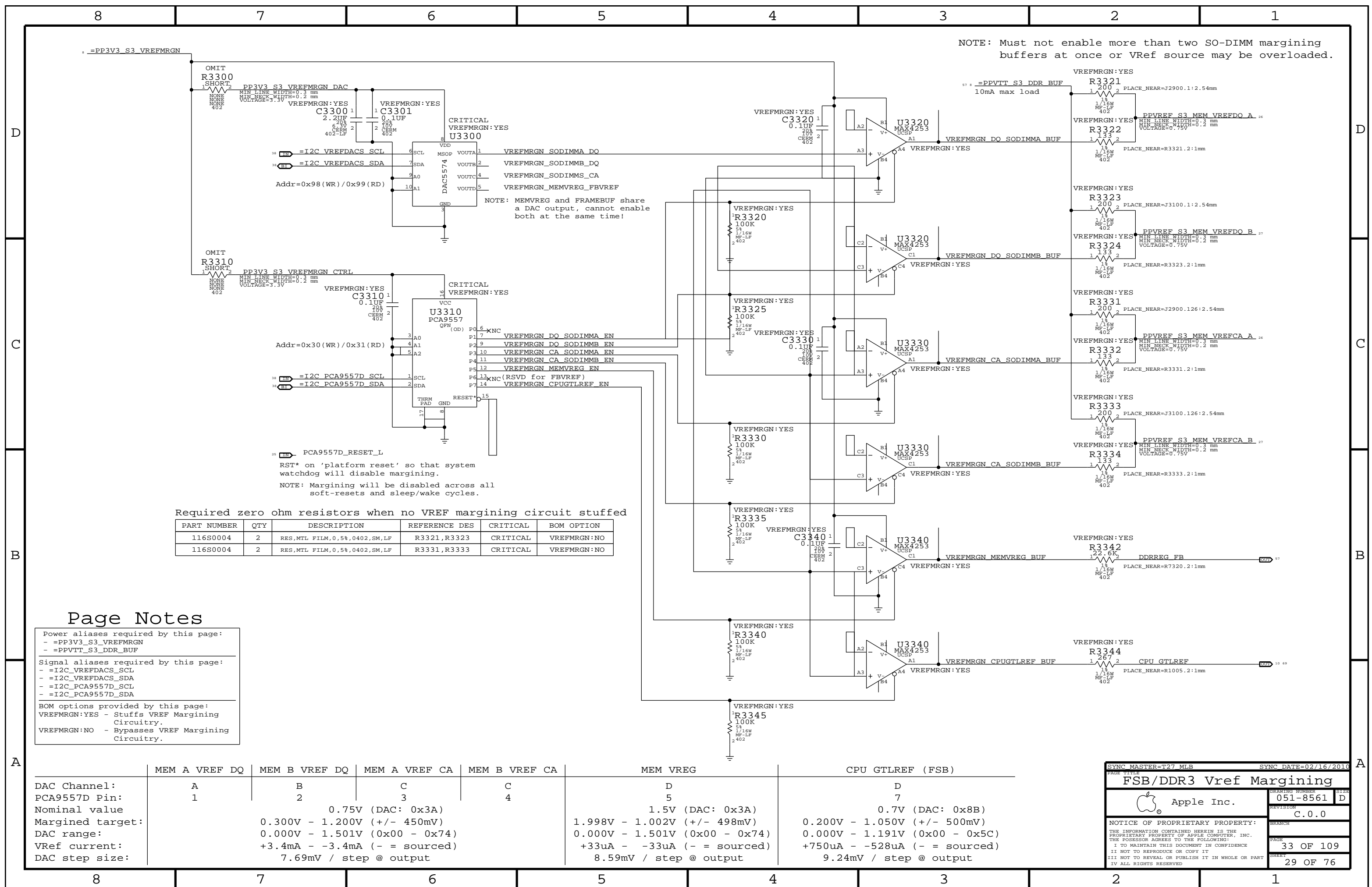
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Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA
```

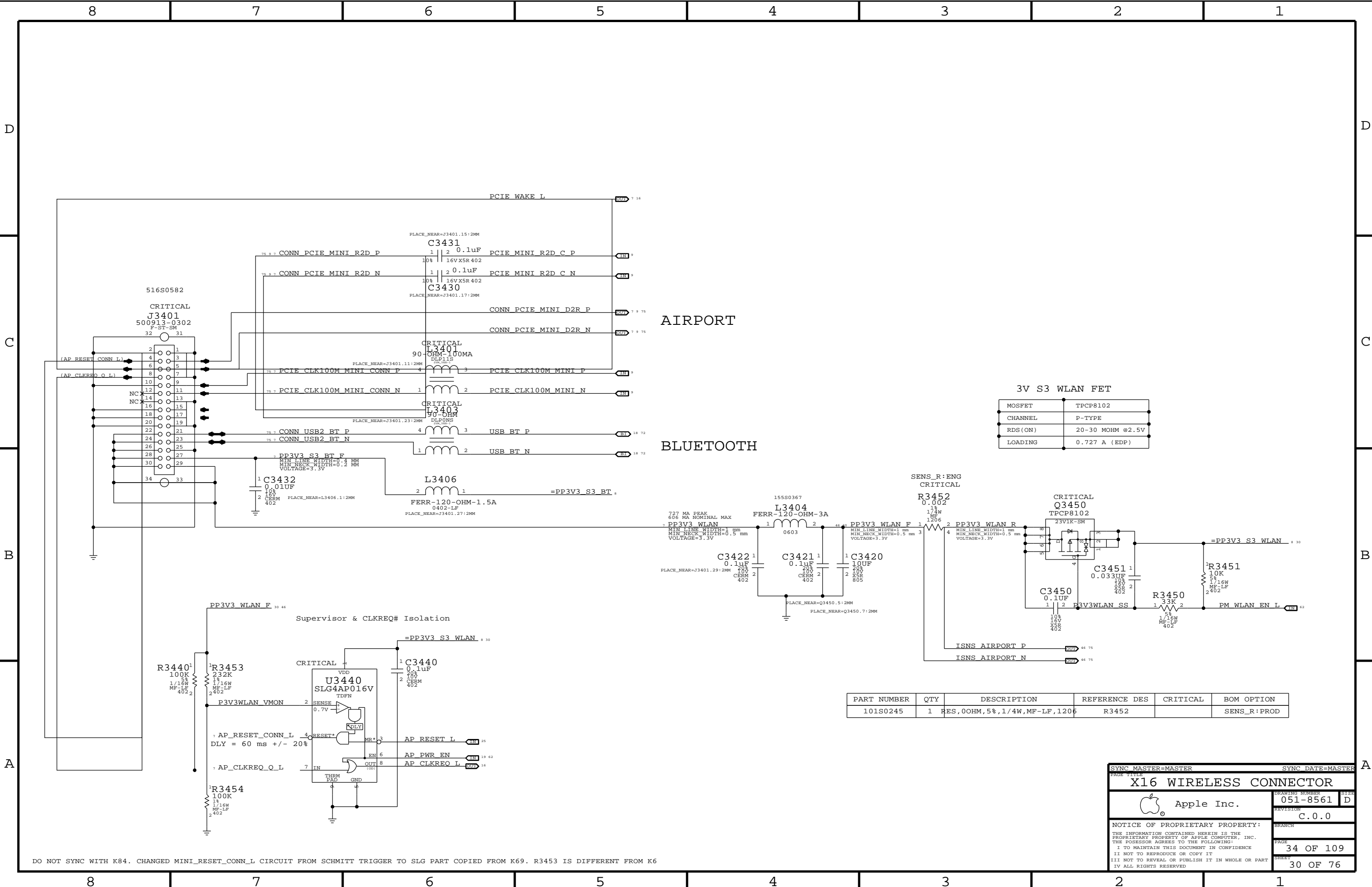
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BOM options provided by this page:
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Proper APN(s) required elsewhere.



[illegible]





AIRPORT

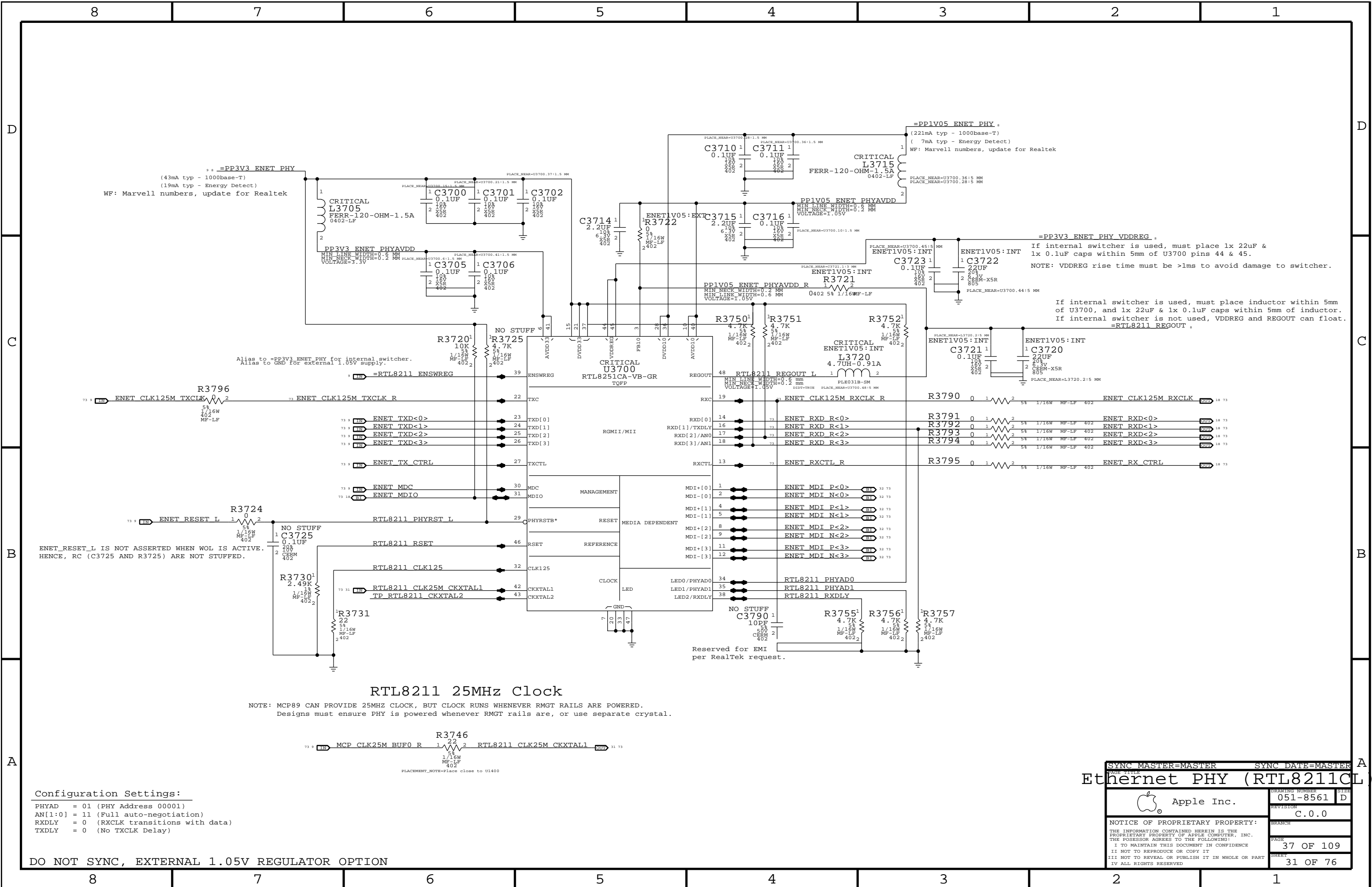
BLUETOOTH

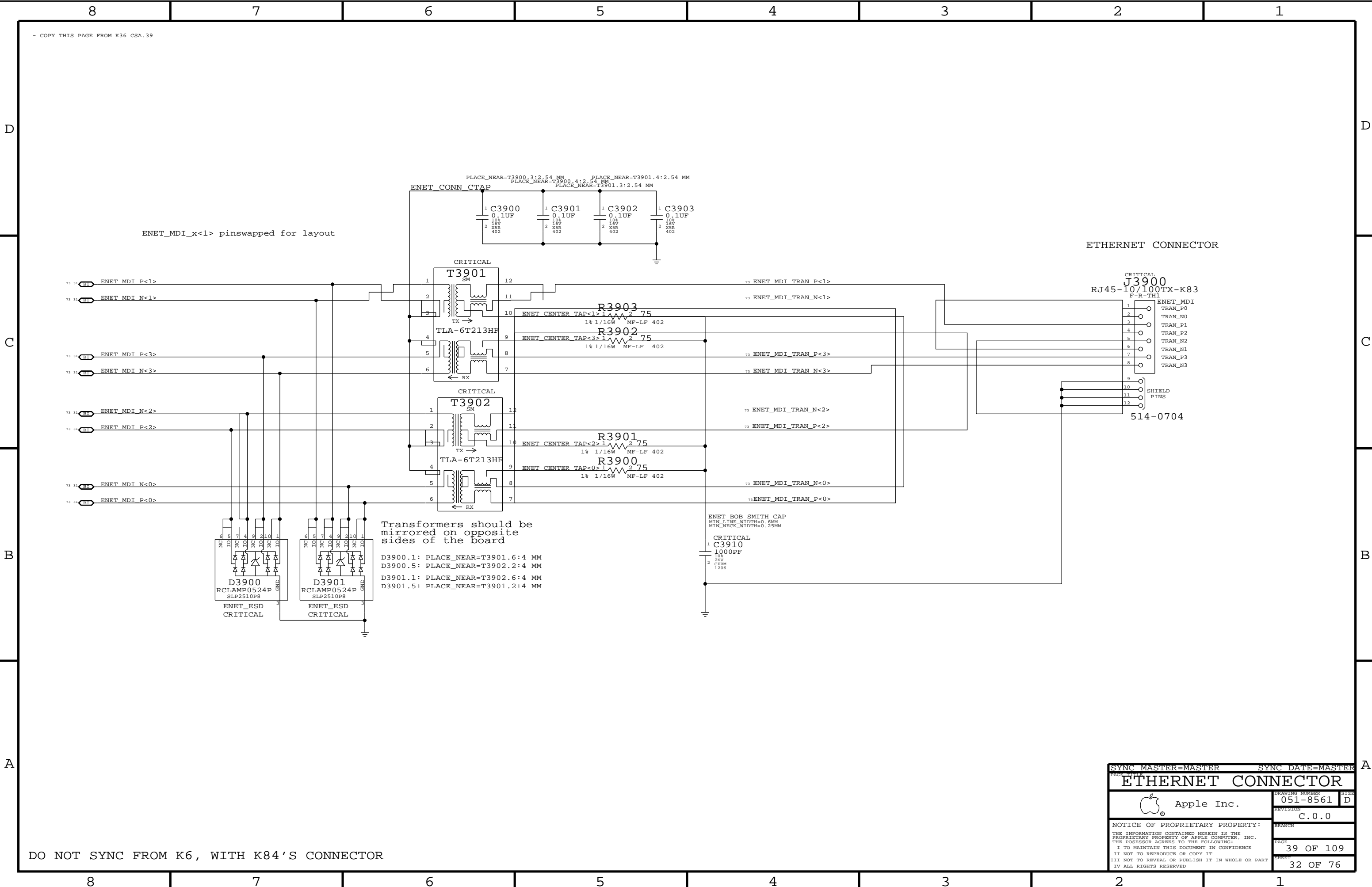
3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (EDP)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
101S0245	1	RES,00HM,5%,1/4W,MF-LF,1206	R3452		SENS_R:PROD

DO NOT SYNC WITH K84. CHANGED MINI_RESET_CONN_L CIRCUIT FROM SCHMITT TRIGGER TO SLG PART COPIED FROM K69. R3453 IS DIFFERENT FROM K6

PAGE TITLE		SYNC DATE=MASTER	
X16 WIRELESS CONNECTOR		DRAWING NUMBER	
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- COPY THIS PAGE FROM K36 CSA.39

ENET_MDI_x<1> pinswapped for layout


ETHERNET CONNECTOR

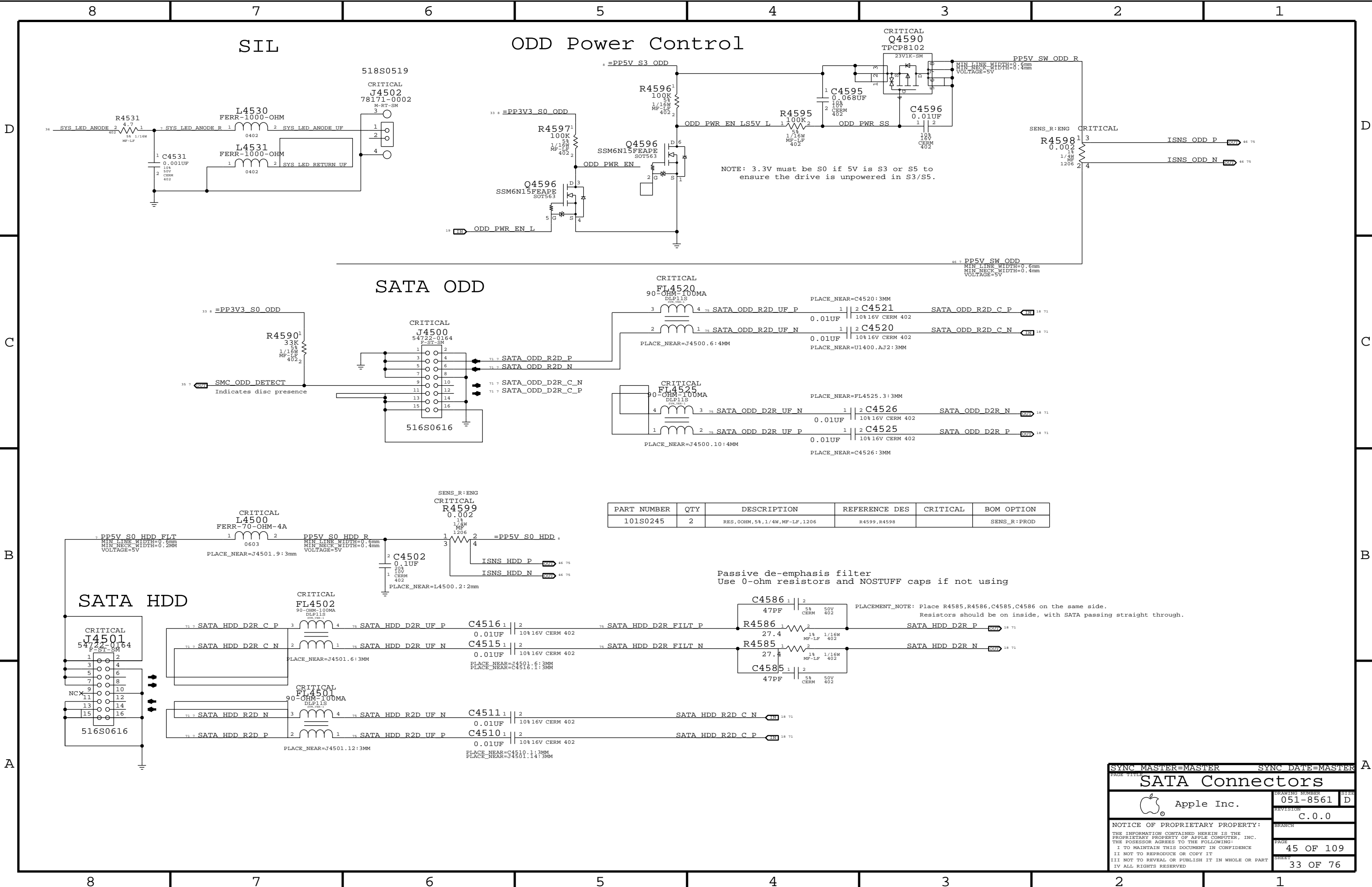
Transformers should be mirrored on opposite sides of the board

D3900.1: PLACE_NEAR=T3901.6:4 MM
D3900.5: PLACE_NEAR=T3902.2:4 MM
D3901.1: PLACE_NEAR=T3902.6:4 MM
D3901.5: PLACE_NEAR=T3901.2:4 MM

ENET_BOB_SMITH_CAP
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
CRITICAL
C3910
1000PF
10V
CERM
1206

DO NOT SYNC FROM K6, WITH K84'S CONNECTOR

PAGE 10/10		PAGE 10/10	
SYNC MASTER=MASTER		SYNC DATE=MASTER	
ETHERNET CONNECTOR			
 Apple Inc.		DRAWING NUMBER	051-8561
		REVISION	C.0.0
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		PAGE	39 OF 109
		SHEET	32 OF 76
		SIZE	D



PAGE TITLE		DRAWING NUMBER		SIZE	
SYNC MASTER=MASTER		051-8561		D	
SYNC DATE=MASTER		REVISION		C.0.0	
SATA Connectors		BRANCH			
Apple Inc.		PAGE		45 OF 109	
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C

B

A

D

C

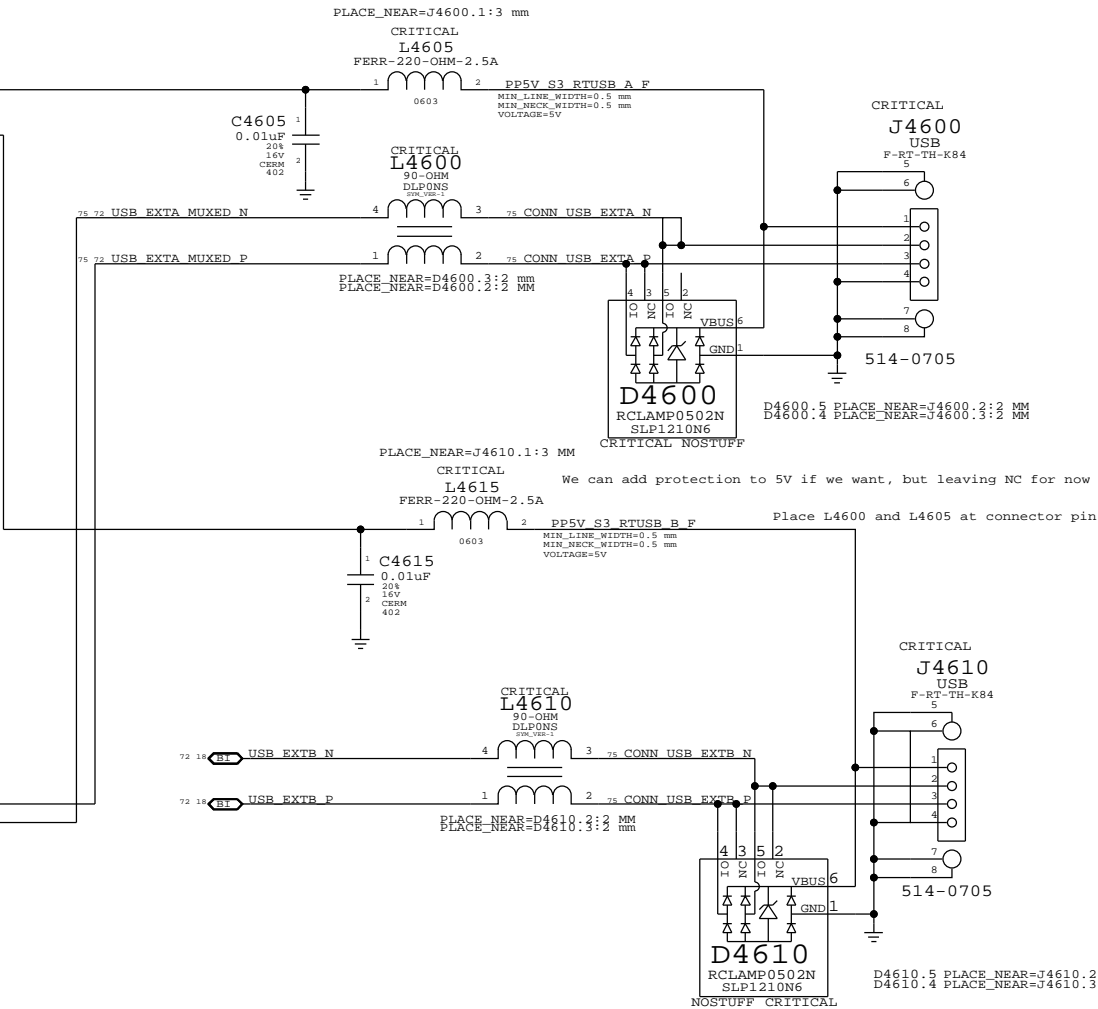
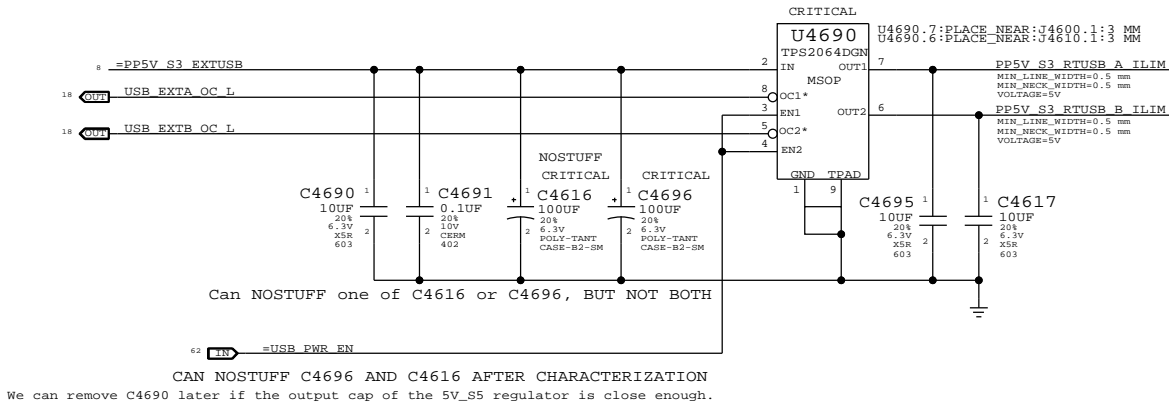
B

A

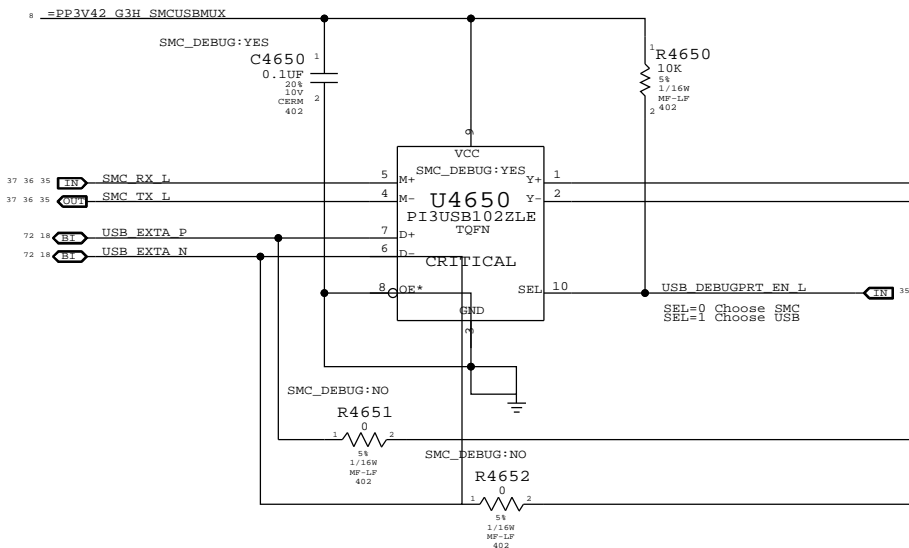
POR IS METAL USB CONNECTOR PARTS

Port Power Switch

USB PORT A (FRONT PORT)




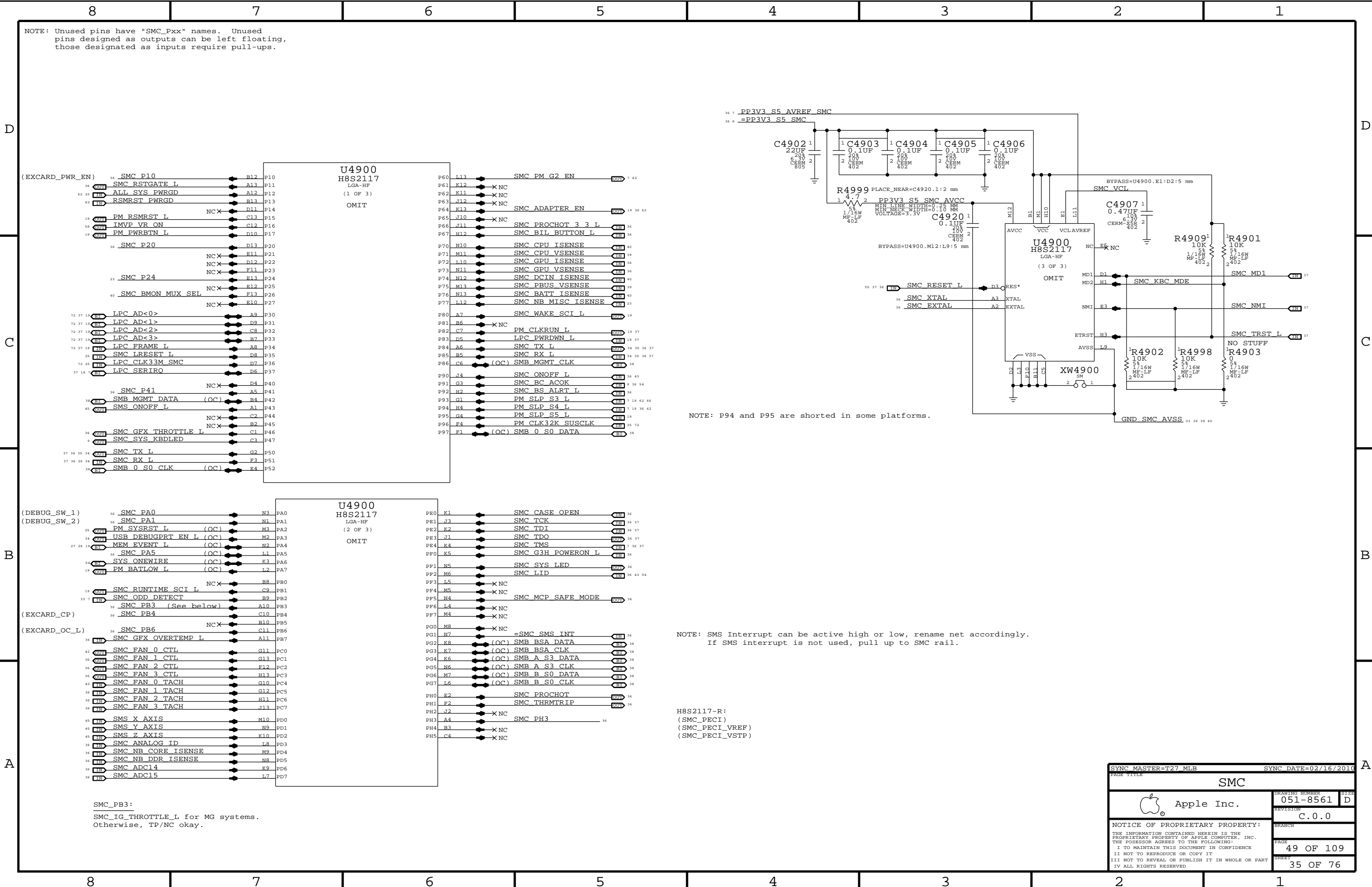
USB/SMC Debug Mux



USB PORT B (BACK PORT)

DO NOT SYNC WITH K84. UPDATED PLACE NEAR NOTES
UPDATED SMC_DEBUG BOMOPTION, STUFFED C4690

SYNC MASTER=(K84_MLB)		SYNC DATE=(10/03/2009)	
PAGE TITLE			
External USB Connectors			
 Apple Inc.		DRAWING NUMBER	051-8561
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B



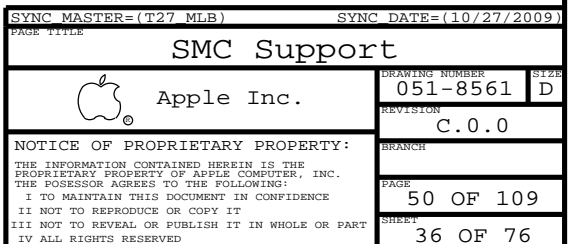
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4

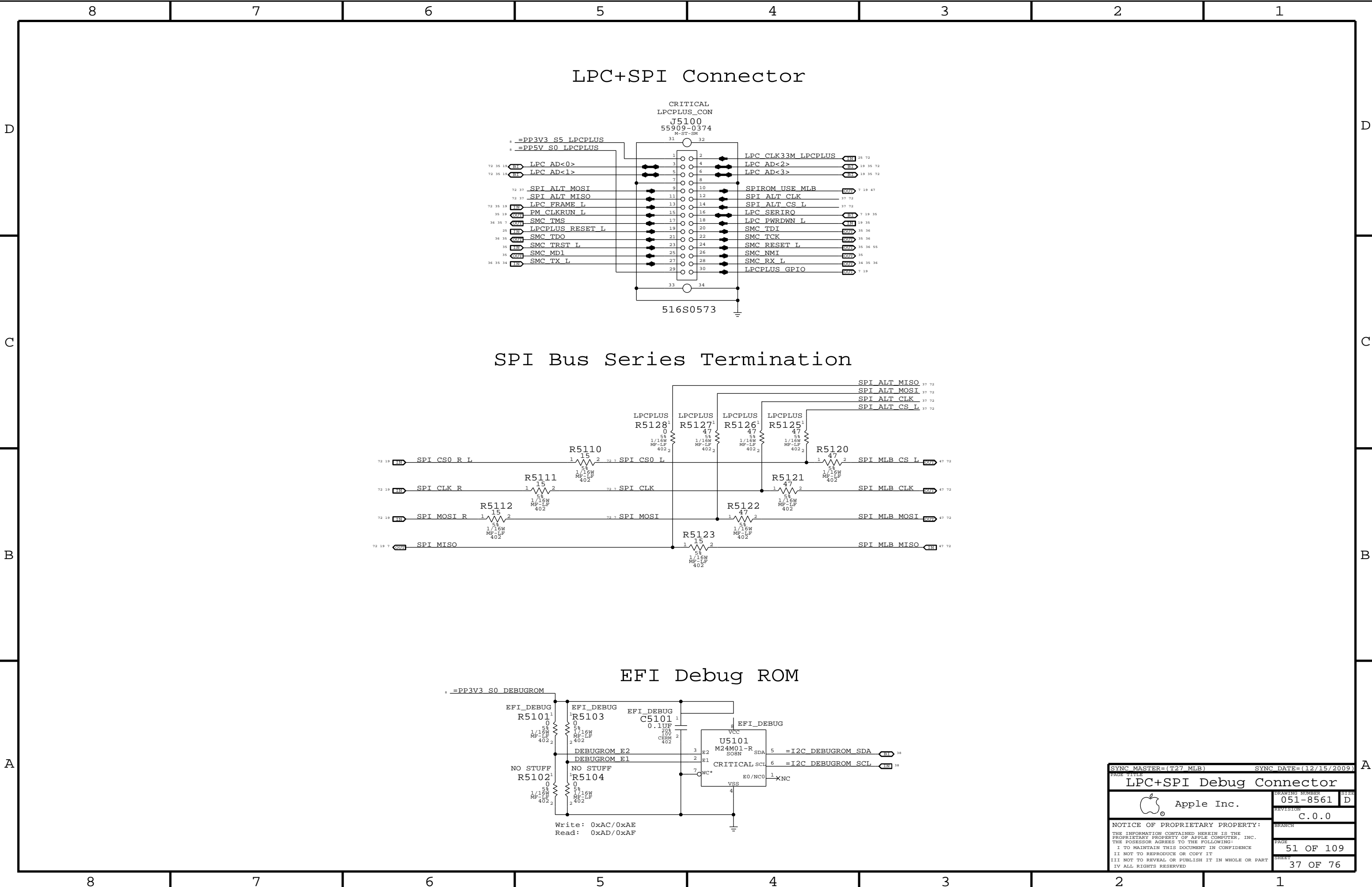


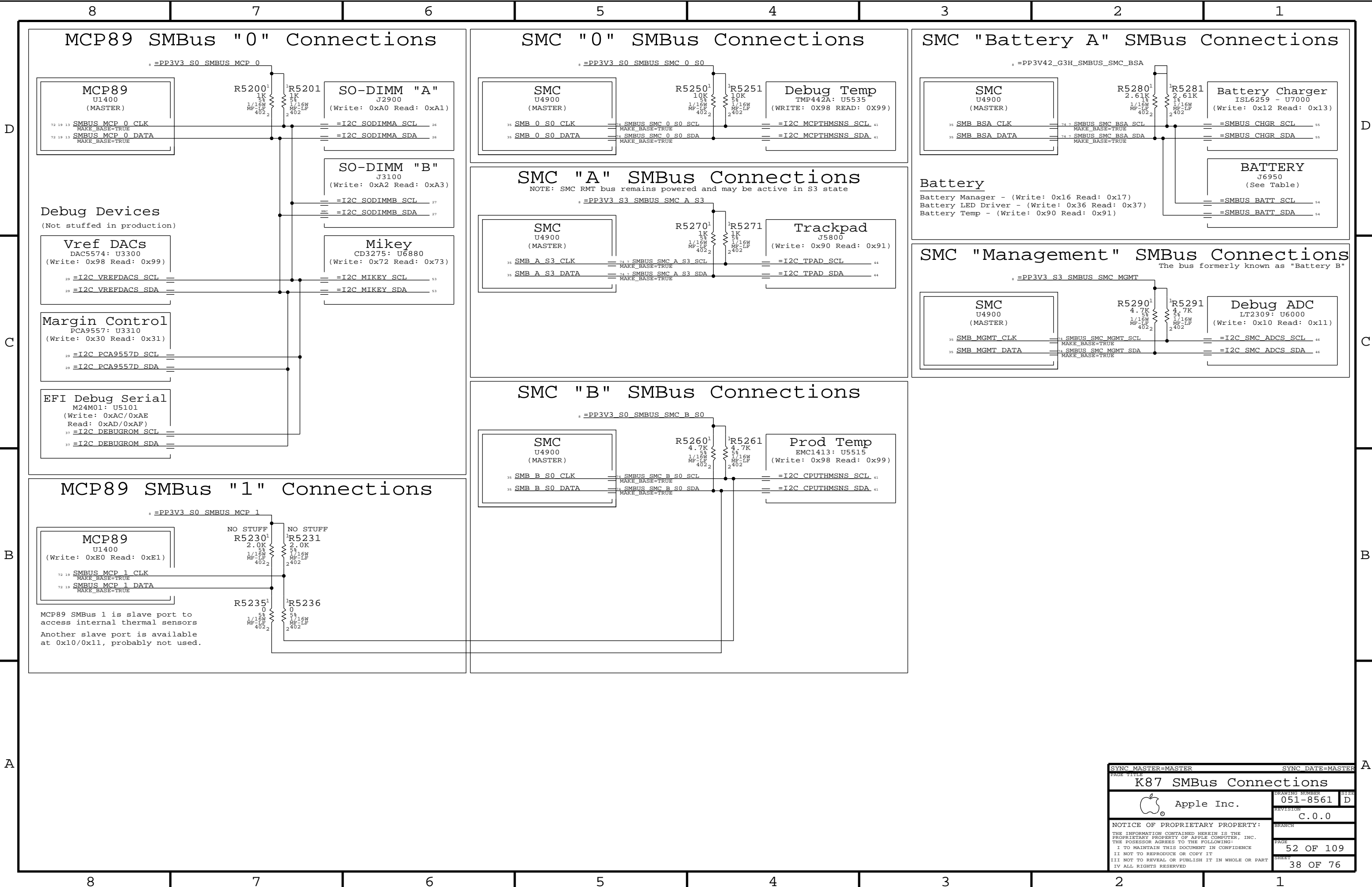
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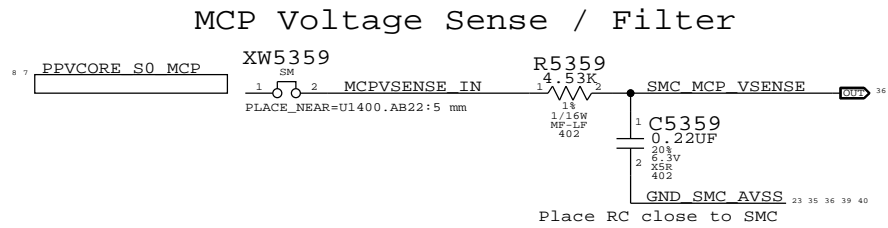
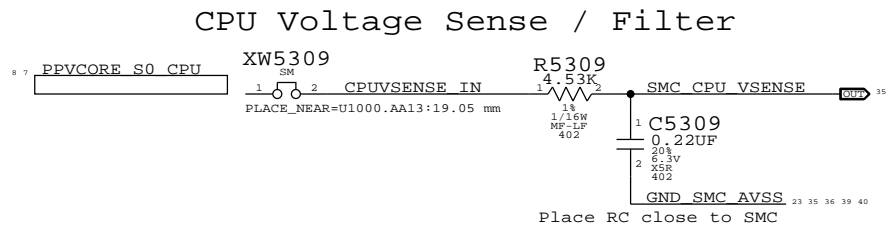




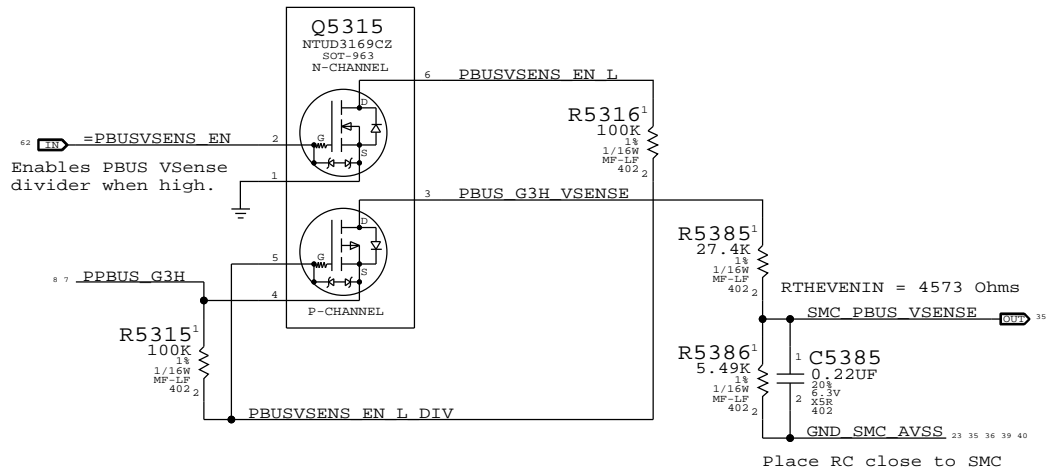
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


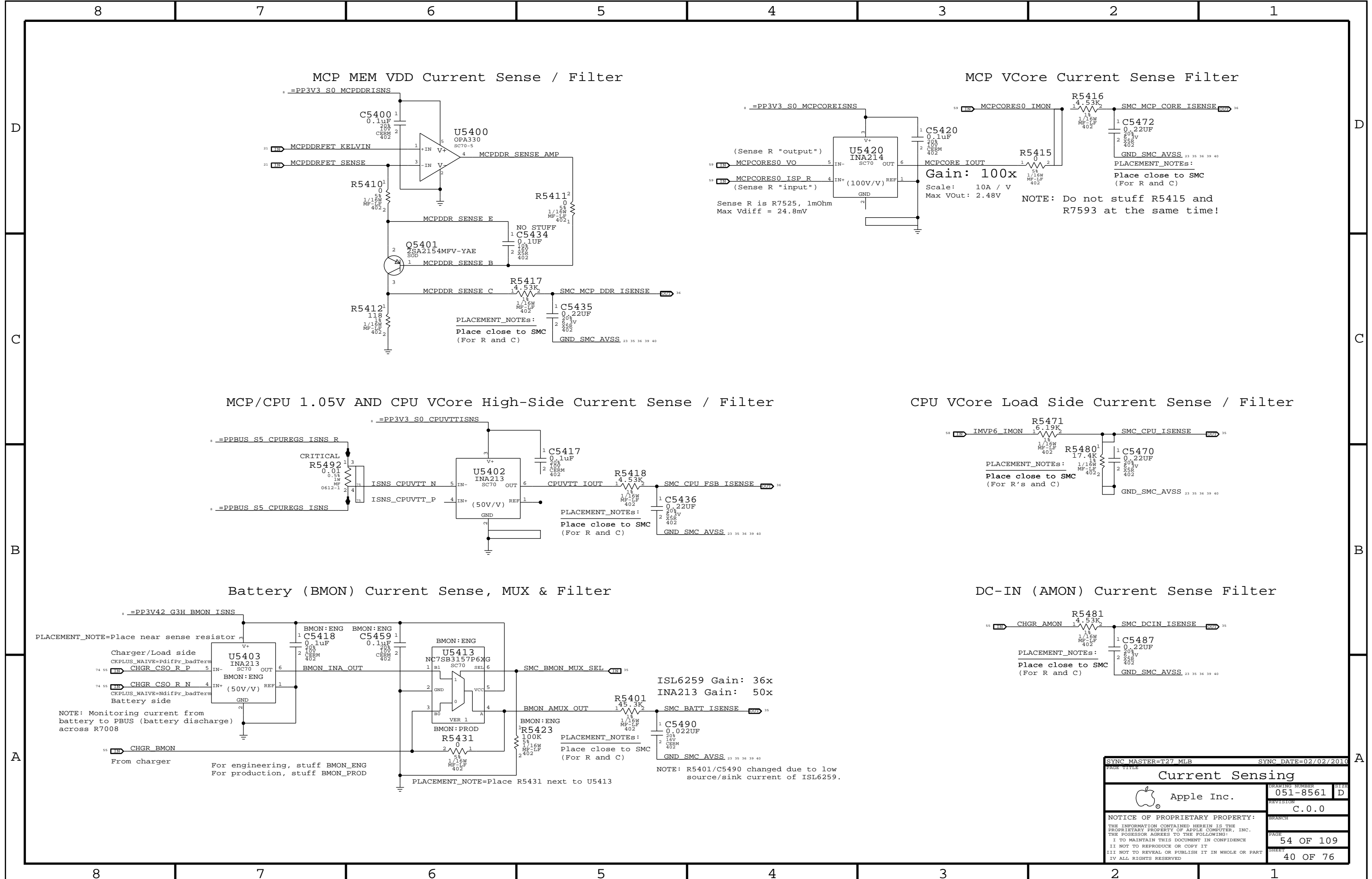




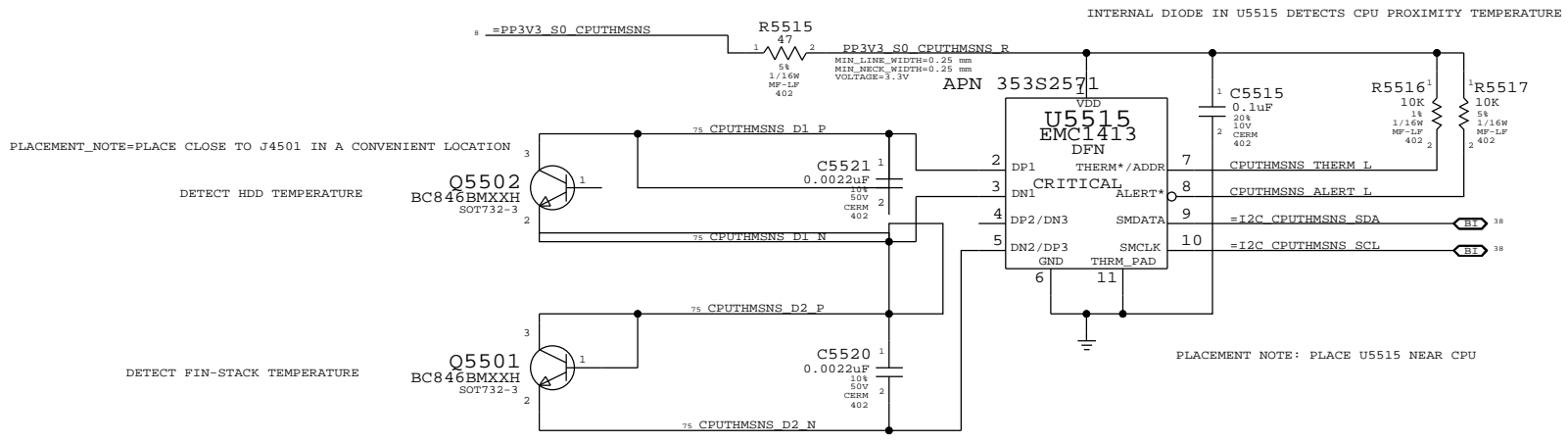
PBUS Voltage Sense Enable & Filter



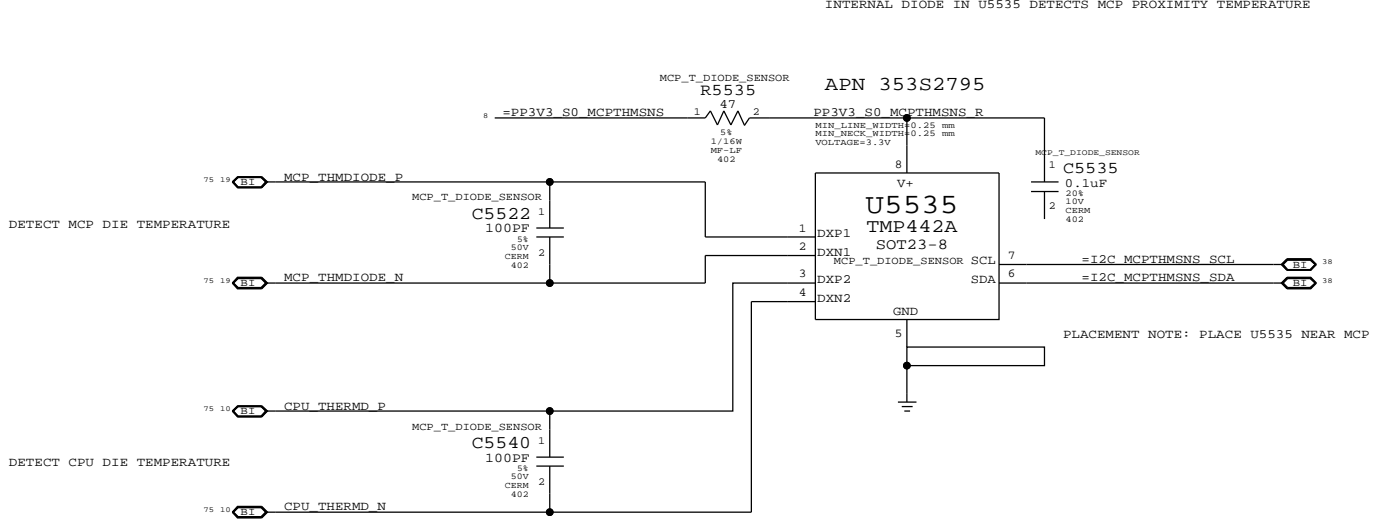
SYNC MASTER=T27_MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
Voltage Sensing			
 Apple Inc.		DRAWING NUMBER	051-8561
		SIZE	D
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


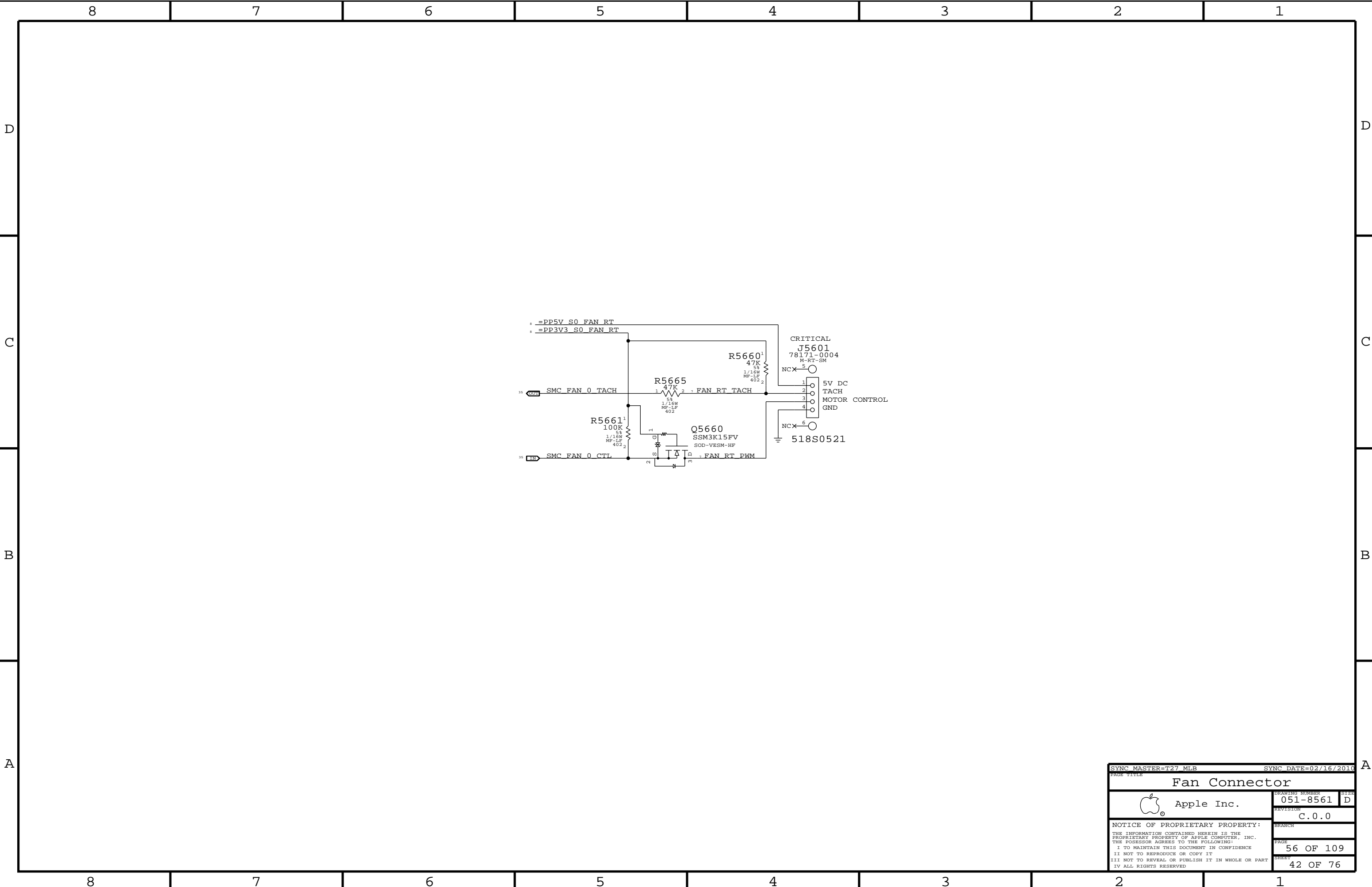
CPU PROXIMITY/HDD FLEX AREA/FINSTACK THERMAL SENSOR




MCP DIE/CPU DIE/MCP PROXIMITY THERMAL SENSOR

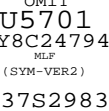


SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
Thermal Sensors		DRAWING NUMBER	
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SYNC MASTER=T27_MLB		SYNC DATE=02/16/2010	
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Fan Connector			
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		PAGE	56 OF 109
		SHEET	42 OF 76

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



BUTTON DISABLE

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA (MAX) 60MA (MAX)	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

43 8 =PP3V3 S3 TPAD

43 8 =PP3V42 G3H TPAD

43 7 WS KBD1

43 7 WS KBD2

43 7 WS KBD3

43 7 WS KBD4

43 7 WS KBD5

43 7 WS KBD6

43 7 WS KBD7

43 7 WS KBD8

43 7 WS KBD9

43 7 WS KBD10

43 7 WS KBD11

43 7 WS KBD12

43 7 WS KBD13

43 7 WS KBD14

7 WS KBD15 CAP

7 WS KBD16 NUM

43 7 WS KBD17

43 7 WS KBD18

43 7 WS KBD19

43 7 WS KBD20

43 7 WS KBD21

43 7 WS KBD22

43 7 WS KBD23

7 WS KBD ONOFF L

43 7 WS LEFT SHIFT KBD

43 7 WS LEFT OPTION KBD

43 7 WS CONTROL KBD

NCX 32

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16

15

14

13

12

11

10

9

8

7

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1

NCX 31

F-RT-SM

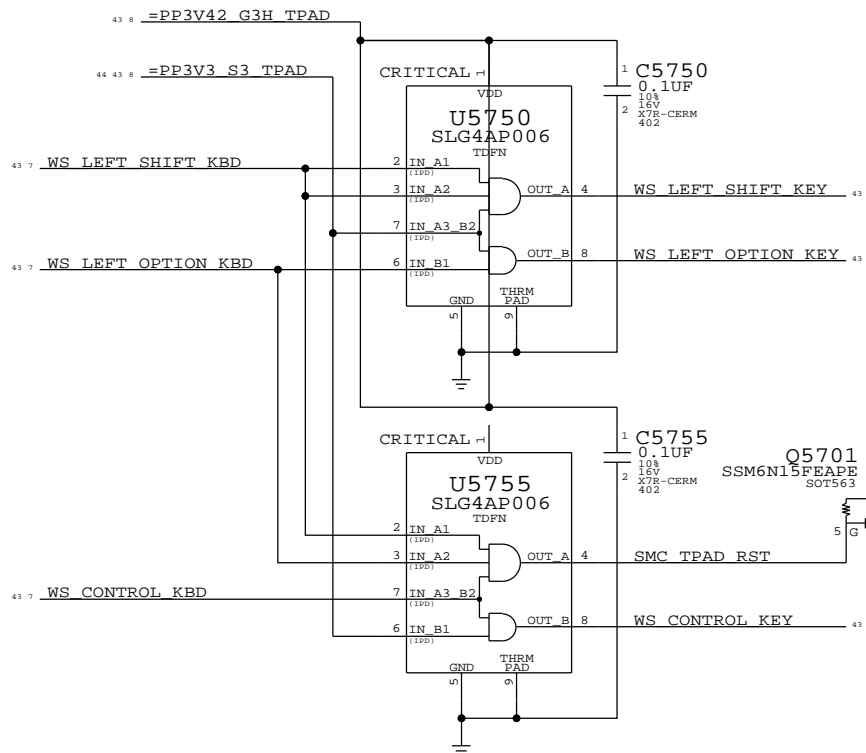
FF14-30A-R11B-B-3H


J5713

CRITICAL

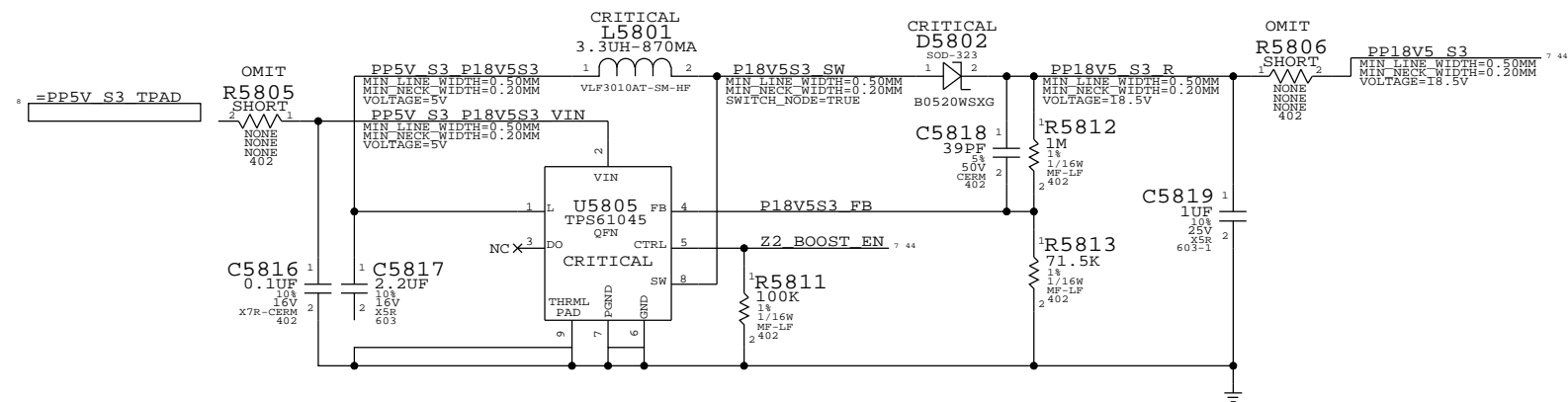
518S0637

Left shift, option & control keys combined with power button cause SMC RESET# assertion. Keys ANDed with PSOC power to isolate when PSOC is not powered.



SYNC MASTER=T27 MLB		SYNC DATE=02/16/2010	
PAGE TITLE			
WELLSPRING 1			
	Apple Inc.	DRAWING NUMBER	051-8561
		SIZE	D
		REVISION	C.0.0
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```
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED
```



CRITICAL
J5800
55560-0228
M-ST-SM

PP3V3 S3 TPAD

PP18V5 S3

Z2 CS L

Z2 DEBUG3

Z2 MOSI

Z2 MISO

Z2 SCLK

Z2 BOOST EN

Z2 HOST INTN

Z2 CLKIN

2

4

6

8

10

12

14

16

18 NCX

20

22

1

3

5

7

9

11

13

15

17

19

21

Z2 KEY ACT L

Z2 RESET

PSOC F CS L

PICKB L

PSOC MISO

PSOC MOSI

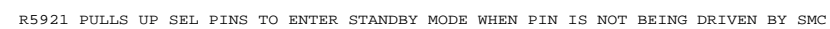
PSOC SCLK

=I2C TPAD SDA

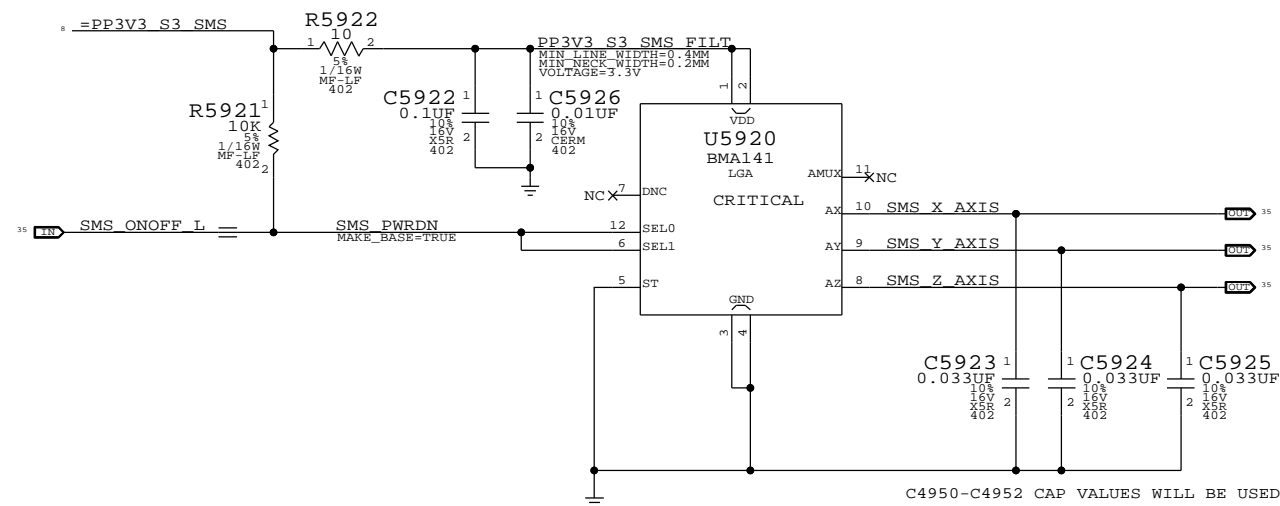
=I2C TPAD SCL

516S0689

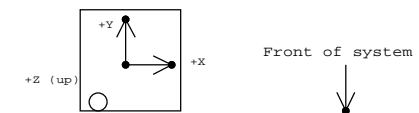
WWW.AliSaler.Com



Analog SMS



Desired orientation when
placed on board top-side:




Circle indicates pin 1 location when placed
in correct orientation

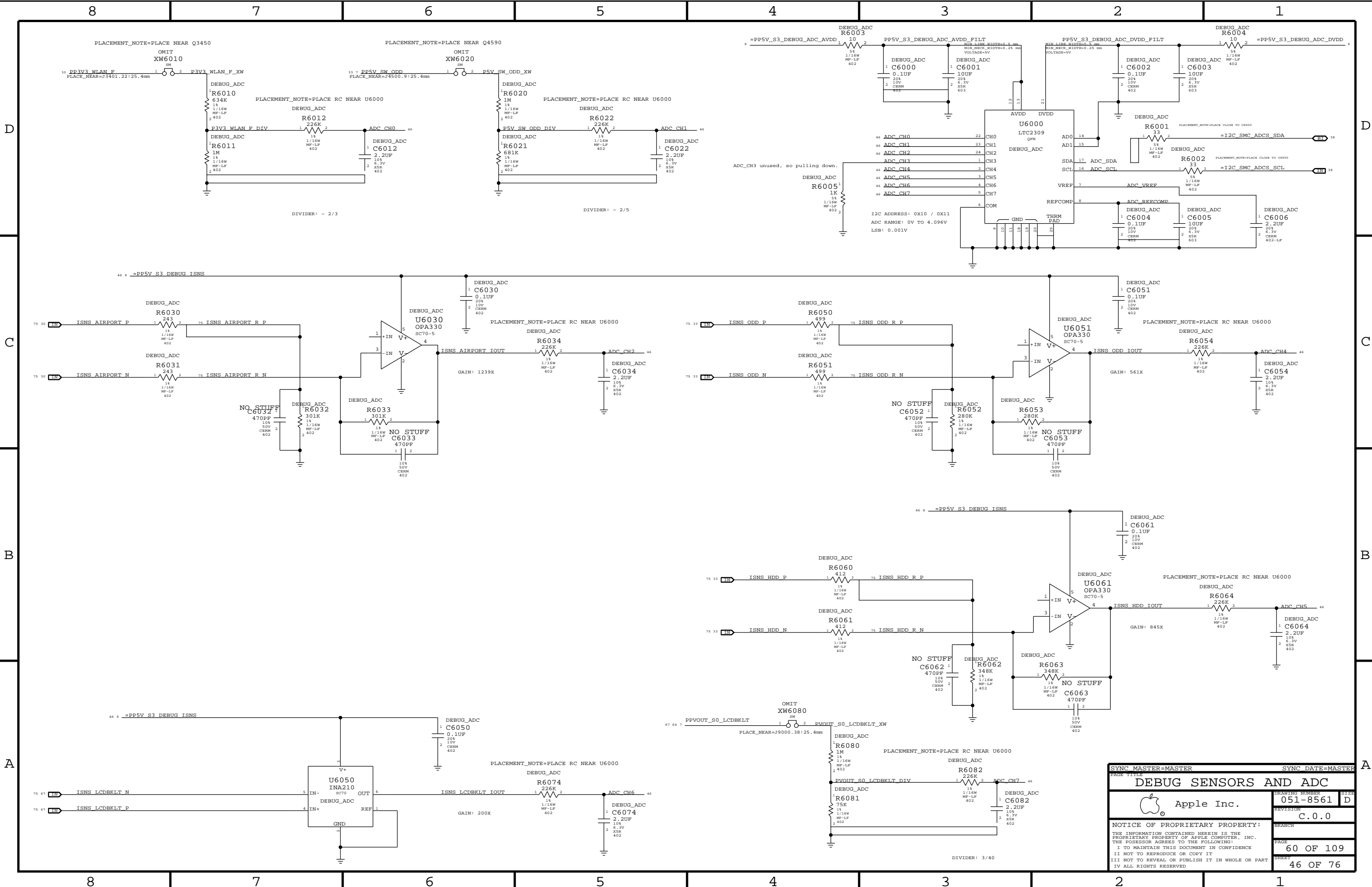
C4950-C4952 CAP VALUES WILL BE USED TO GET CUT-OFF FREQUENCY OF ~146HZ


PLACE_NEARs:

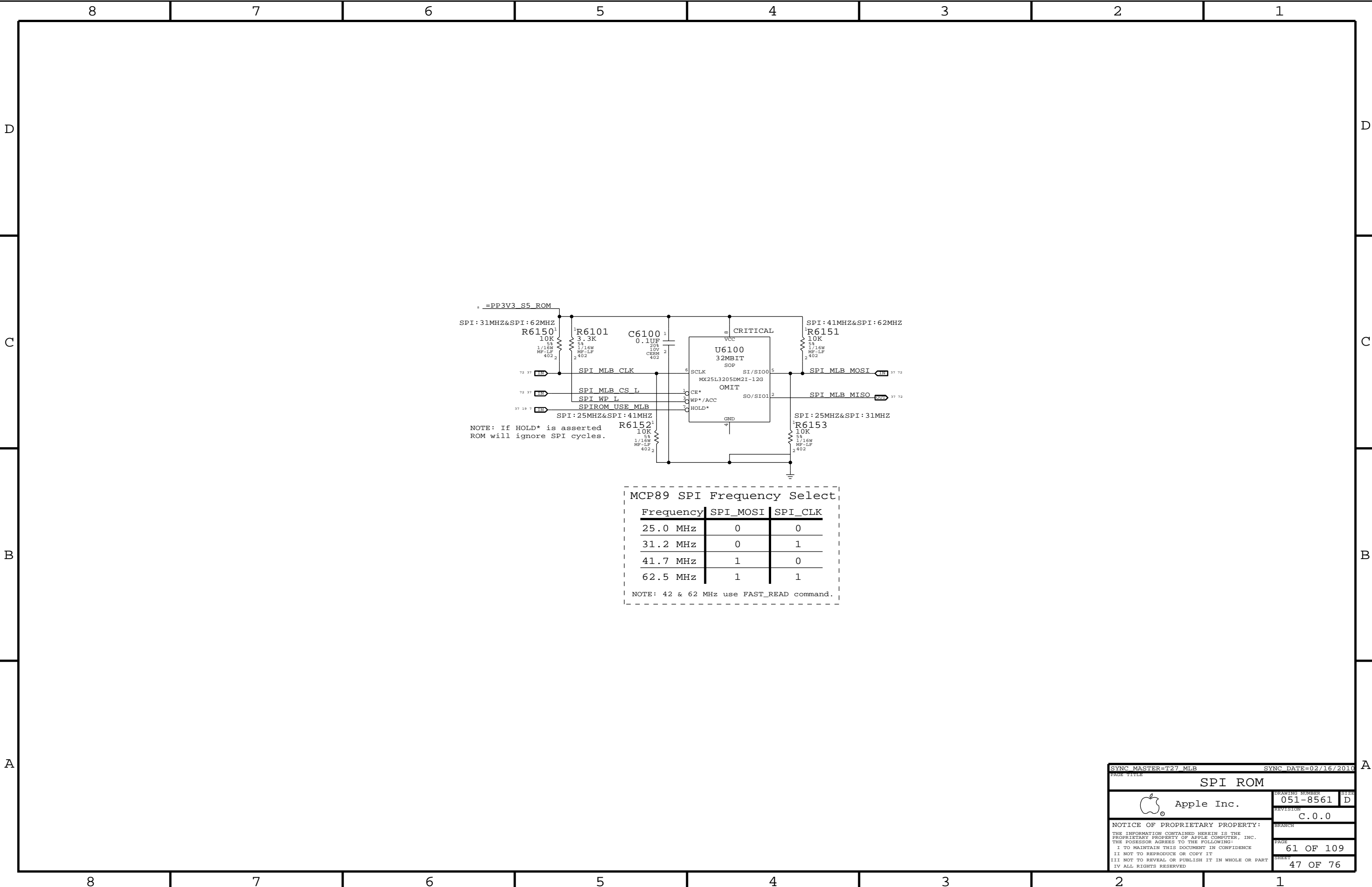
C5923.1:PLACE_NEAR=U4900.M10:2.54MM
C5924.1:PLACE_NEAR=U4900.N9:2.54MM
C5925.1:PLACE_NEAR=U4900.K10:2.54MM

DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923,C5924,C5925. ADDED PLACE NEARS

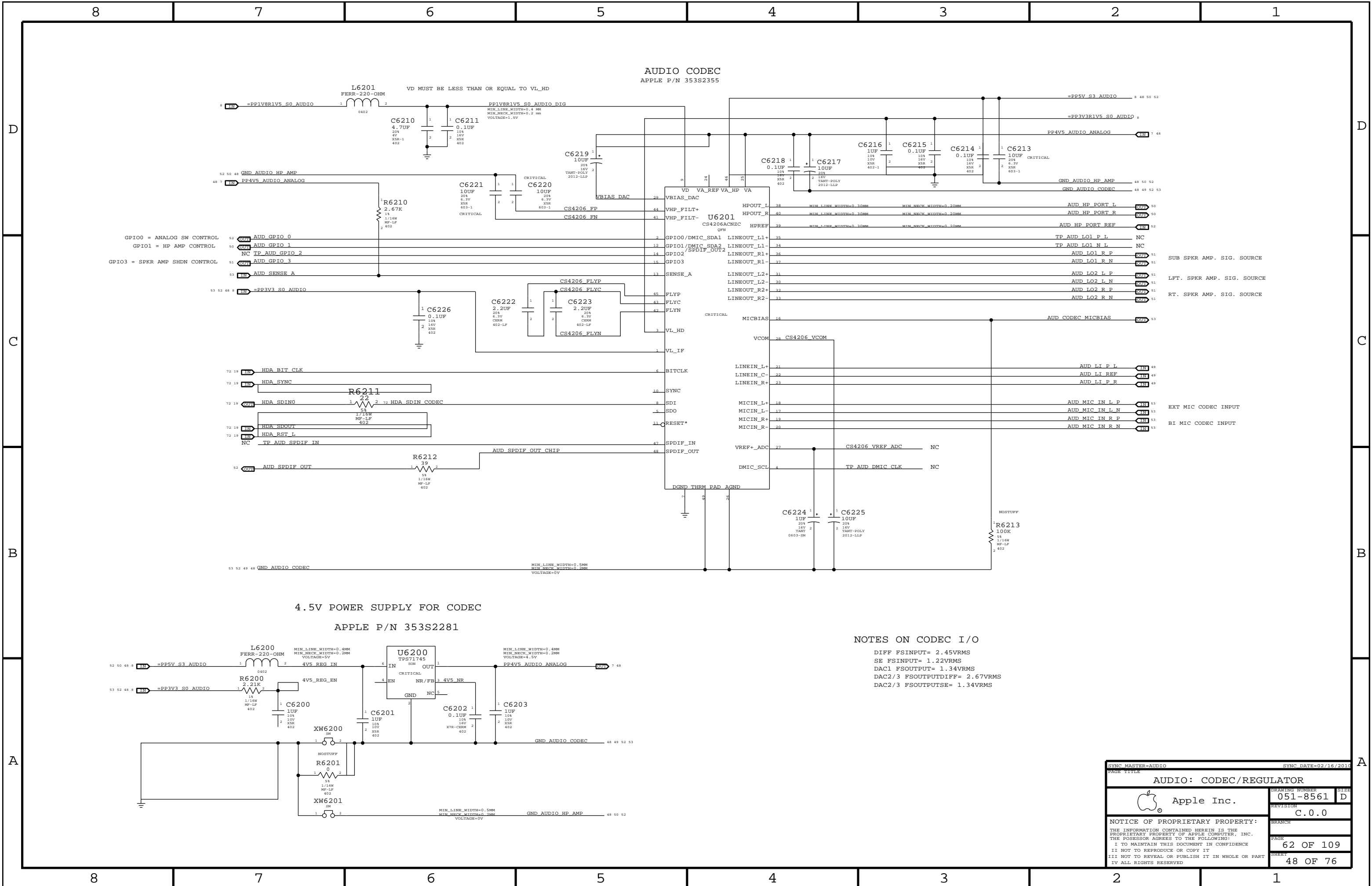
SYNC MASTER-MASTER		SYNC DATE-MASTER	
PAGE TITLE			
SMS			
 Apple Inc.	DRAWING NUMBER	SIZE	
	051-8561	D	
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	BRANCH		
	PAGE	59 OF 109	
	SHEET	45 OF 76	




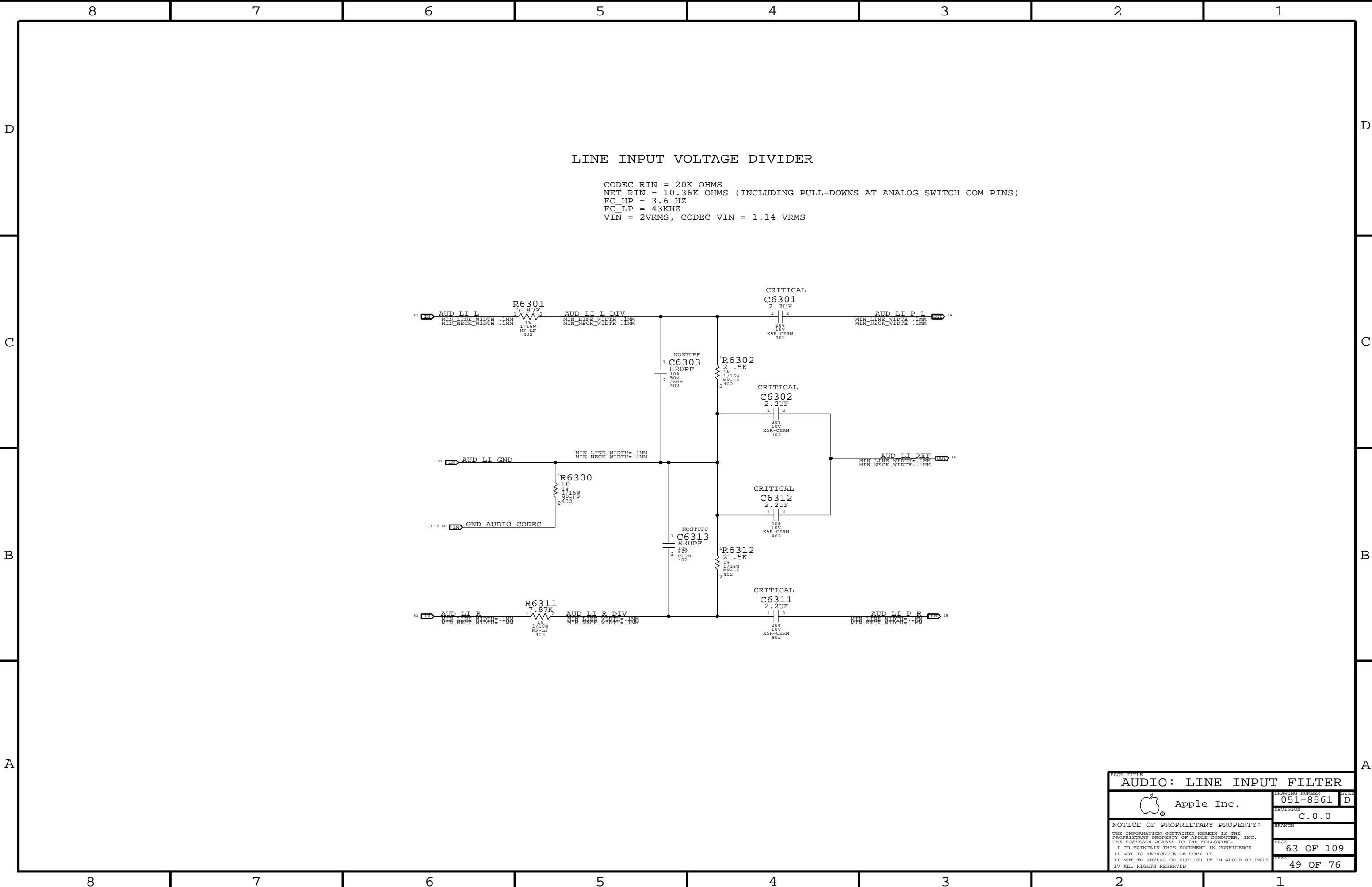
SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
DEBUG SENSORS AND ADC			
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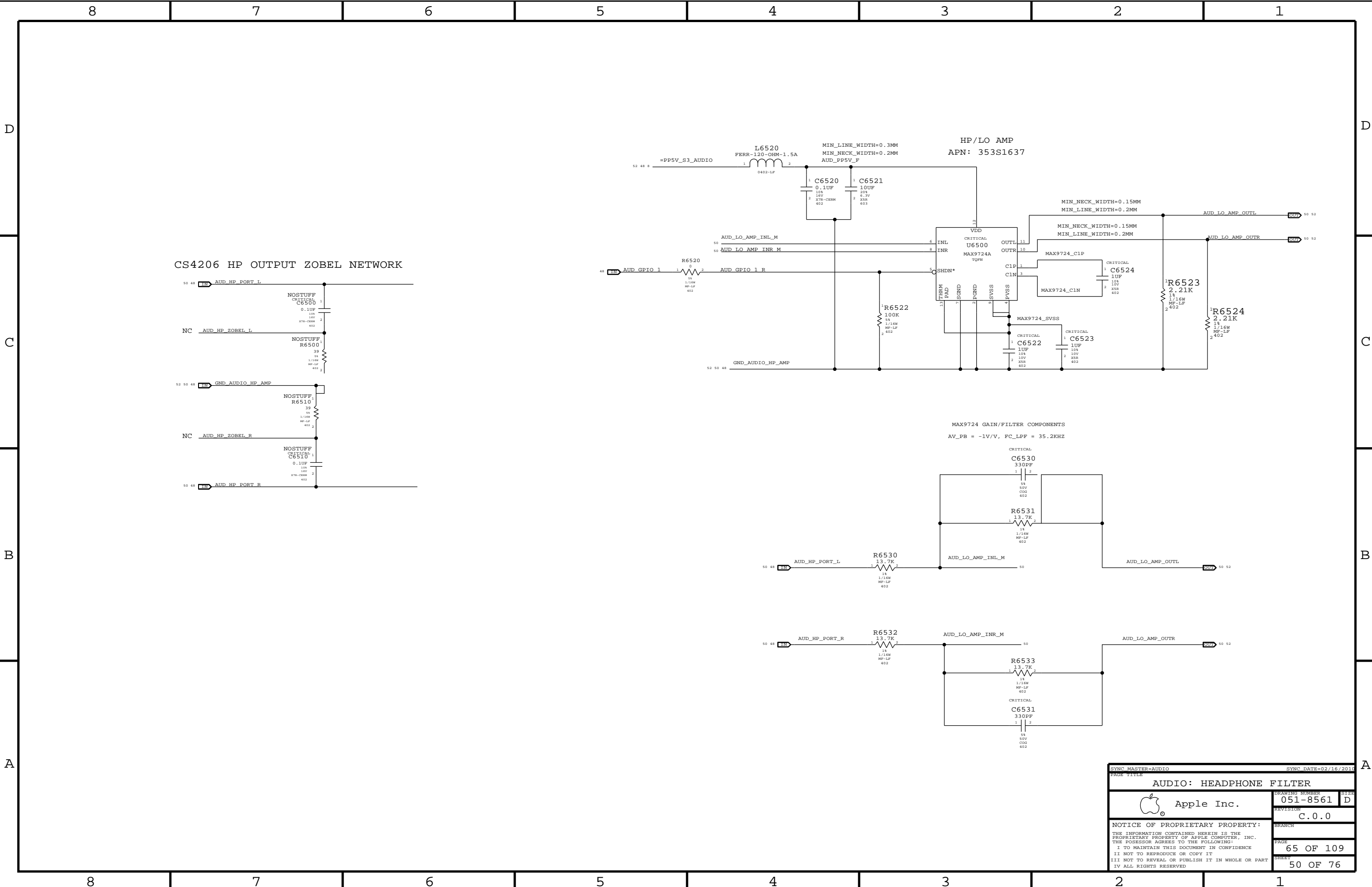



MCP89 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
25.0 MHz	0	0
31.2 MHz	0	1
41.7 MHz	1	0
62.5 MHz	1	1
NOTE: 42 & 62 MHz use FAST_READ command.		



SYNC MASTER=AUDIO		SYNC DATE=02/16/2010	
PAGE TITLE			
AUDIO: CODEC/REGULATOR			
 Apple Inc.	DRAWING NUMBER	051-8561	SIZE
	REVISION	C.0.0	D
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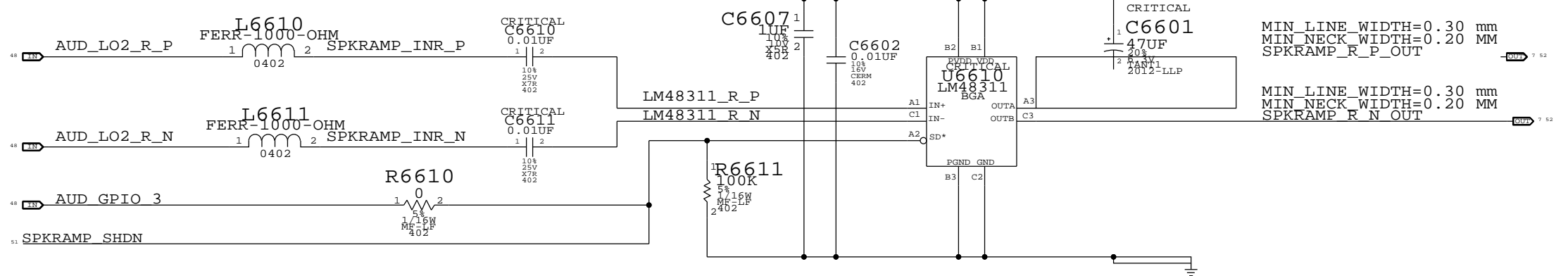
SYNC MASTER=AUDIO		SYNC DATE=02/16/2010	
PAGE TITLE			
AUDIO: HEADPHONE FILTER		DRAWING NUMBER	
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		BRANCH	
		PAGE	
		65 OF 109	
		SHEET	
		50 OF 76	

SATELLITE 796Hz < HPF FC < 936Hz
SUB 80 Hz < HPF FC < 94 Hz
GAIN 6DB (2V/V)
SPRK AMP. INPUT REFERRED CLIP POINT = ~-6dBFS

ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

51 8 =PP5V_S3_AUDIO_AMP

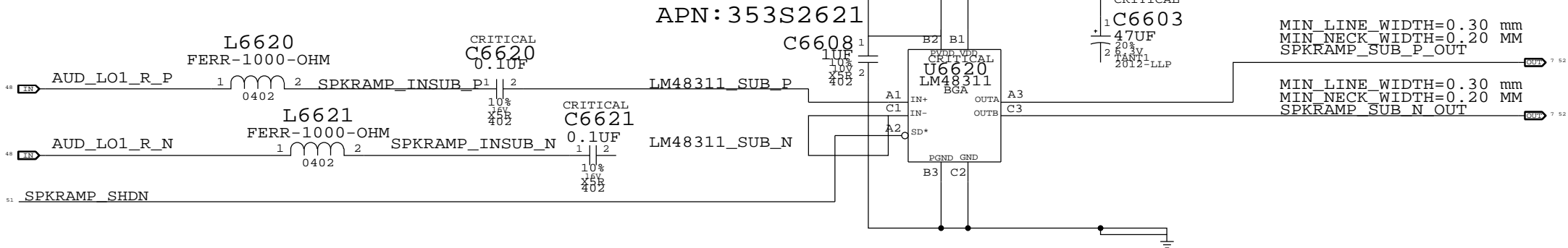
APN: 353S2621



ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

51 8 =PP5V_S3_AUDIO_AMP

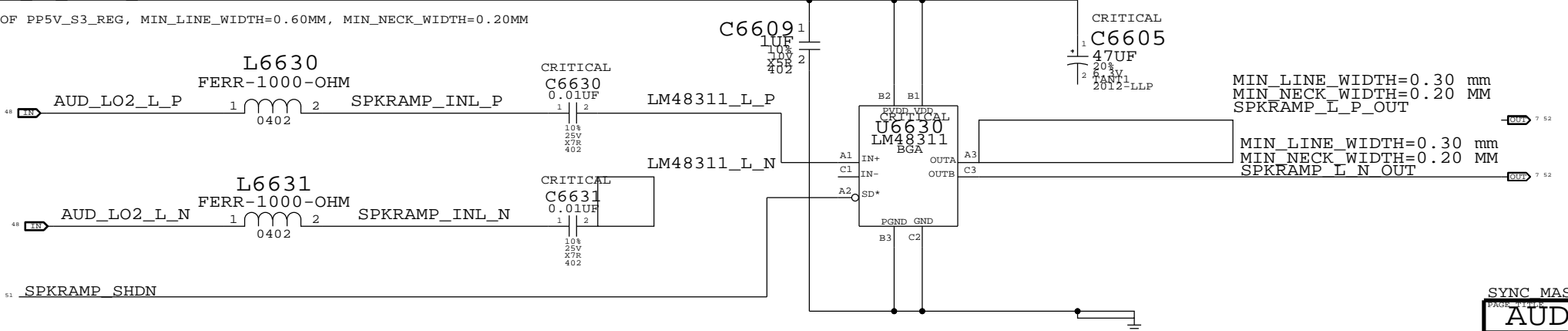
APN: 353S2621




51 8 =PP5V_S3_AUDIO_AMP

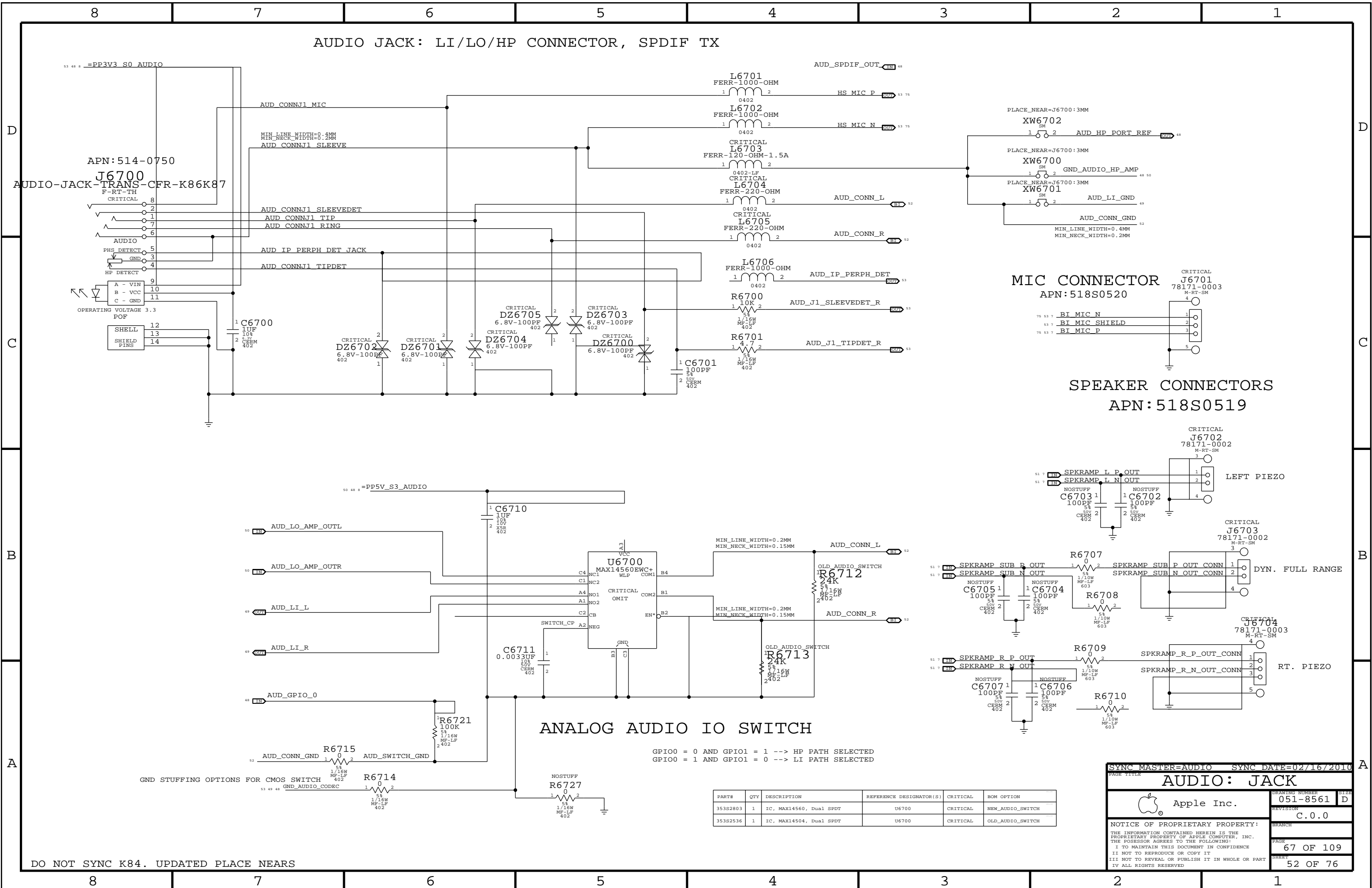
ALIAS OF PP5V_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

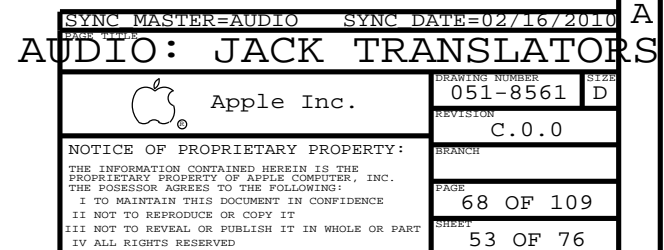
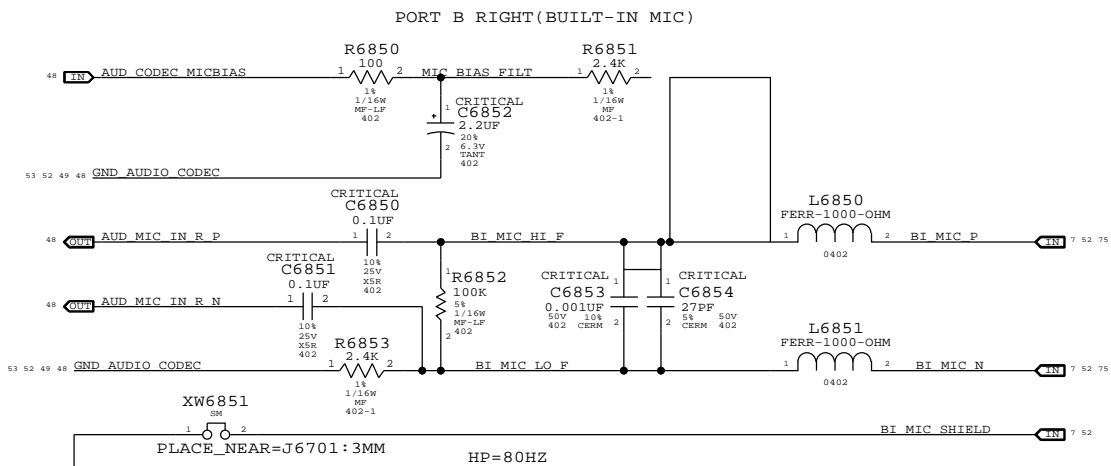
APN: 353S2621

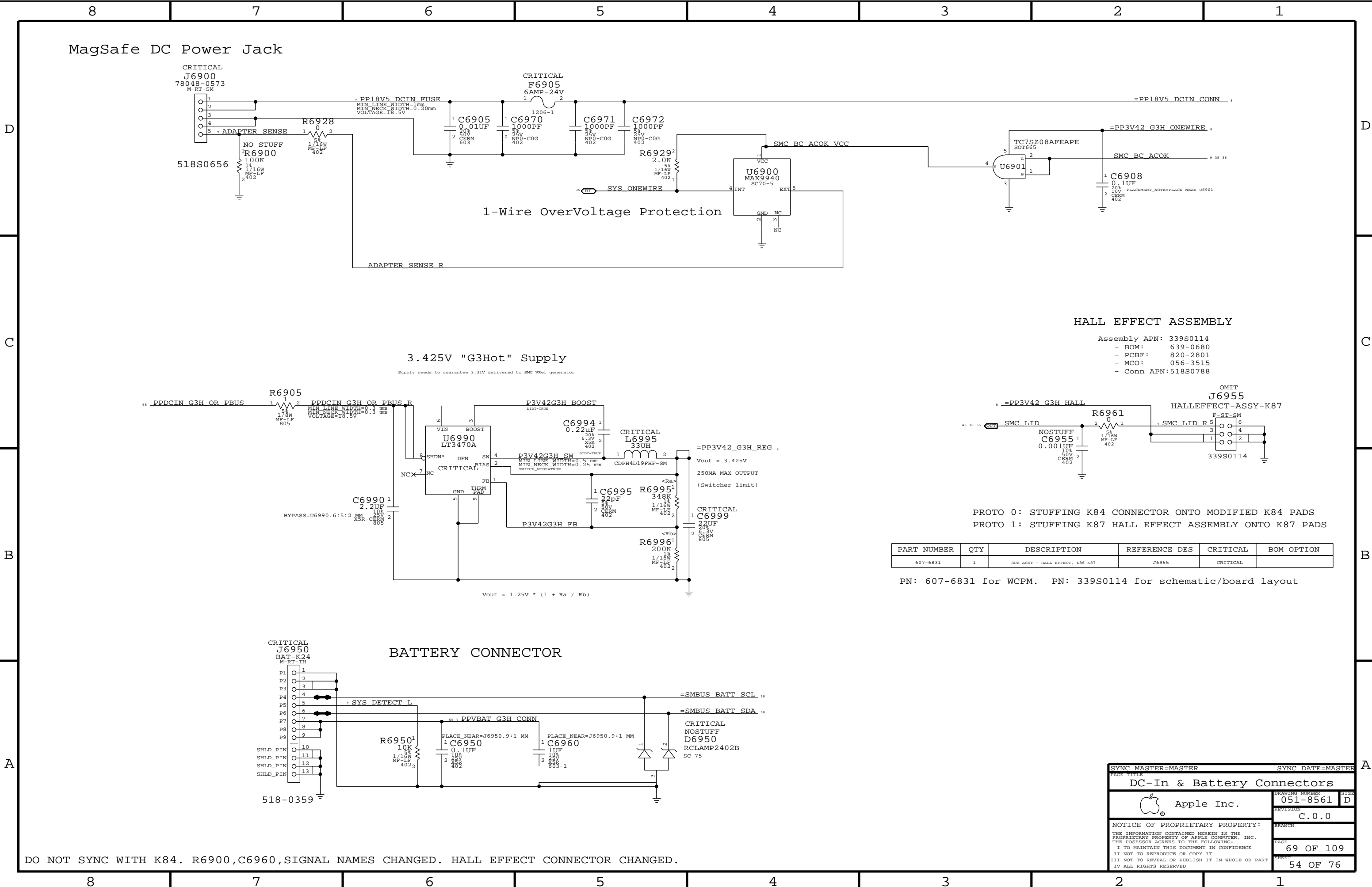


SYNC MASTER=AUDIO SYNC DATE=02/16/2010

AUDIO0: SPEAKER AMP		
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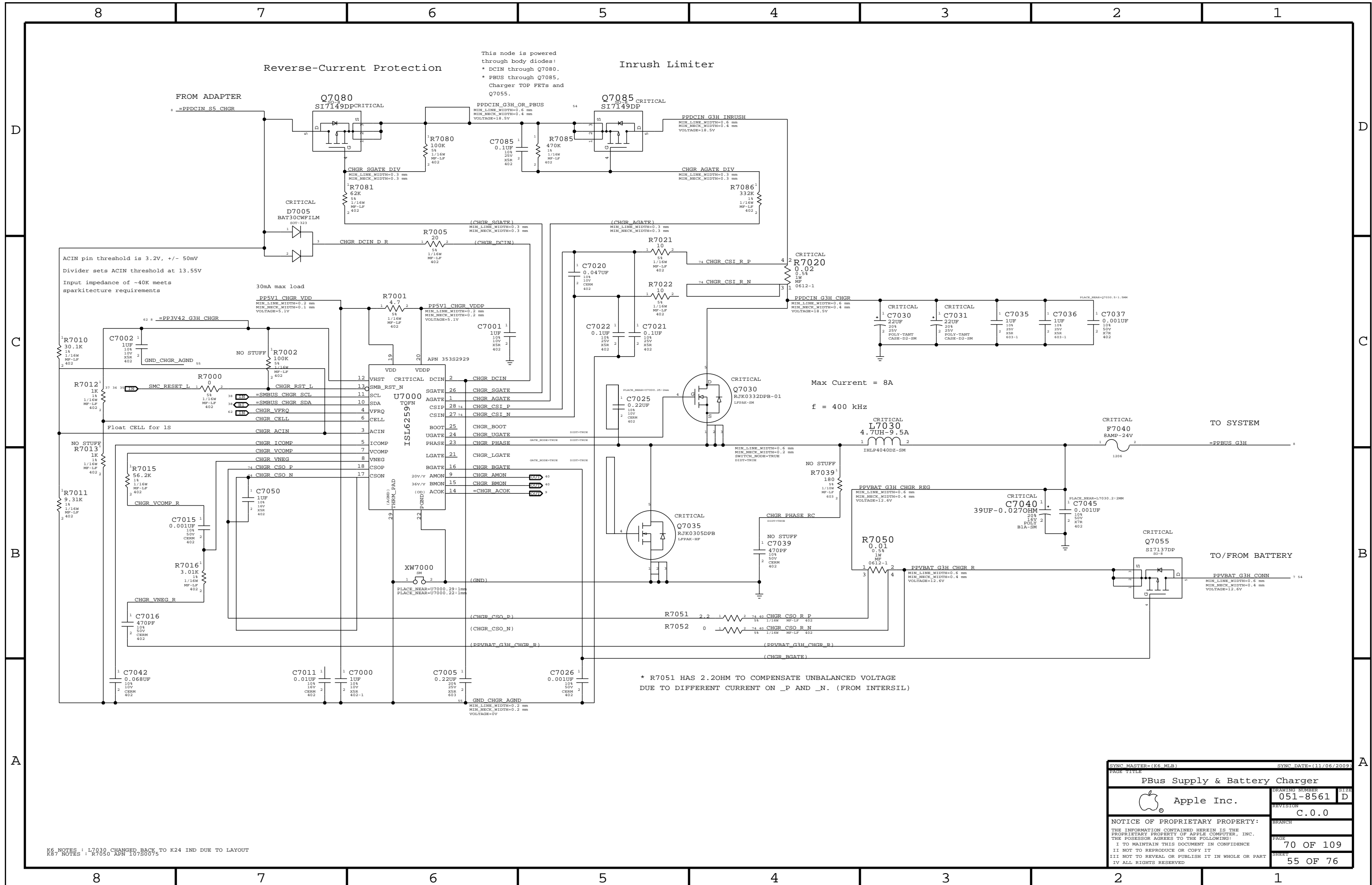


DCB




PAGE TITLE		PAGE TITLE	
DC-In & Battery Connectors		DC-In & Battery Connectors	
Apple Inc.		DRAWING NUMBER	051-8561
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DO NOT SYNC WITH K84. R6900,C6960,SIGNAL NAMES CHANGED. HALL EFFECT CONNECTOR CHANGED.



K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT
K87 NOTES : R7050 APN 10750075

SYNC MASTER=(K6 MLB)		SYNC DATE=(11/06/2009)	
PAGE TITLE			
PBus Supply & Battery Charger			
 Apple Inc.	DRAWING NUMBER	051-8561	SIZE D
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5V_S3 / 3.3V_S5 POWER SUPPLY

$$V_{OUT} = (2 * R_A / R_B) + 2$$

$$V_{OUT} = (2 * R_C / R_D) + 2$$

ROUTING NOTE:
Place XW7203 by Pin1 OF L7260.

ROUTING NOTE:
Place XW7202 by C7292.

ROUTING NOTE:
Place XW7204 by Pin 2 of L7220.

ROUTING NOTE:
Place XW7205 by C7252.

ROUTING NOTE:
Place XW7201 between Pin 15 and Pin 25 of U7200.

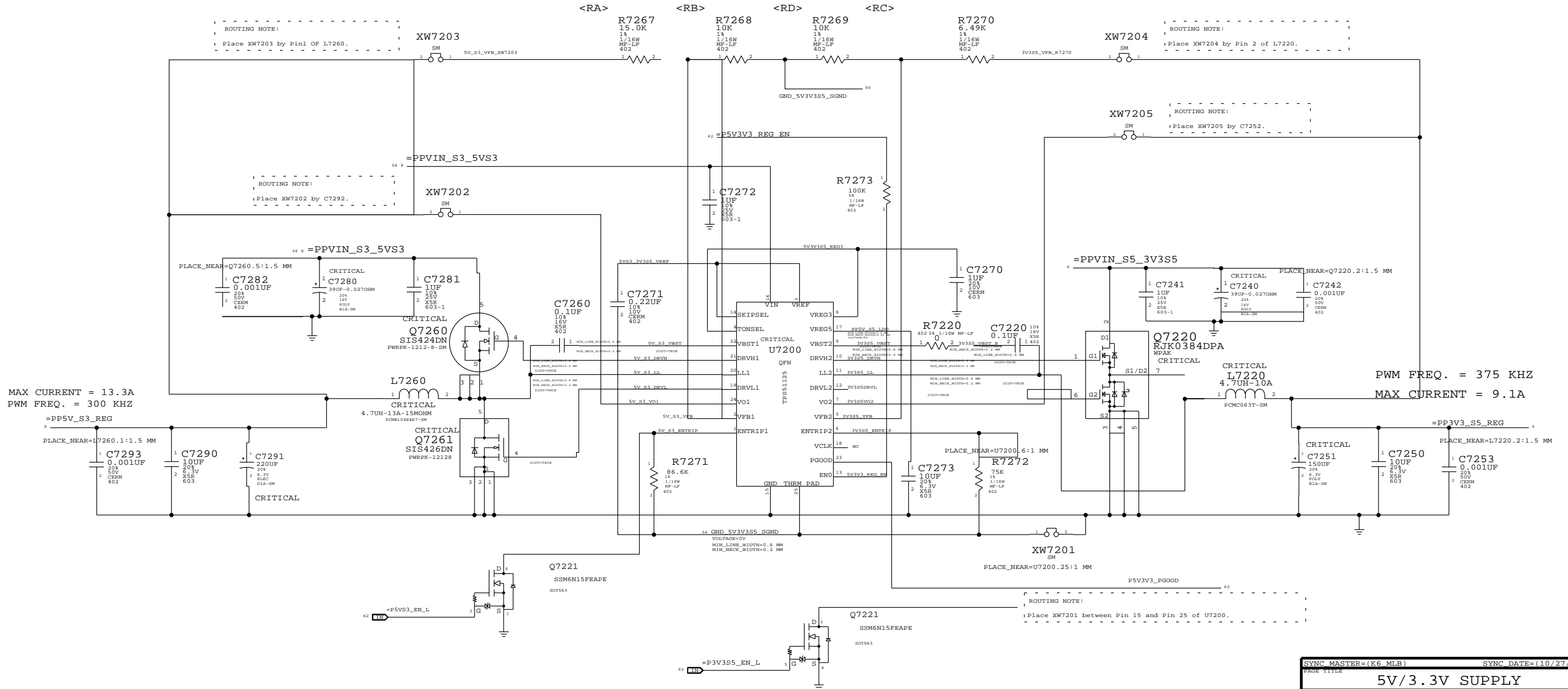
MAX CURRENT = 13.3A
PWM FREQ. = 300 KHZ

PWM FREQ. = 375 KHZ
MAX CURRENT = 9.1A


SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.

NOTE: DONT SYNC THIS PAGE FROM T27

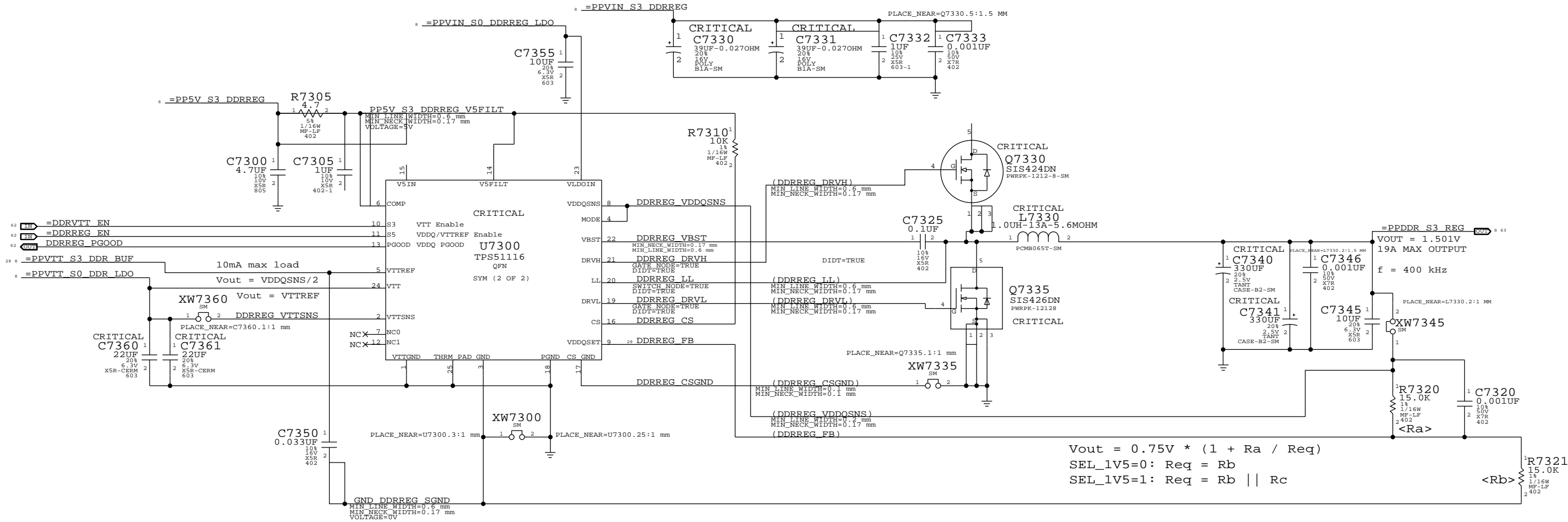
SYNC MASTER=(K6 MLB)		SYNC DATE=(10/27/2009)			
PAGE TITLE					
5V/3.3V SUPPLY					
Apple Inc.	DRAWING NUMBER		051-8561		
	REVISION		C.0.0		
	PAGE		72 OF 109		
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$$V_{OUT} = (2 * RC / RD) + 2$$


SEPERATED MASTER PGOOD FOR BOTH 5V AND 3V3.


SYNC MASTER=(K6 MLB)		SYNC DATE=(10/27/2009)	
PAGE TITLE			
5V/3.3V SUPPLY			
		DRAWING NUMBER 051-8561	
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1.5V/0.75 DDR3 POWER SUPPLY



$$V_{out} = 0.75V * (1 + R_a / R_{eq})$$
$$SEL_{1V5}=0: R_{eq} = R_b$$
$$SEL_{1V5}=1: R_{eq} = R_b || R_c$$

NOTE: DONT SYNC THIS PAGE FROM T27. C7330 AND C7331 IS CHANGED TO OSCON CAPS
NOTE: DONT SYNC THIS PAGE FROM K6 REMOVED R7380

SYNC MASTER=(K6 MLB)		SYNC DATE=(11/06/2009)	
PAGE TITLE			
1.5V/0.75V DDR3		SUPPLY	
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		REVISION	C.0.0
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[illegible][illegible]

IMVP6 CPU VCore REGULATOR

DPRSLPVR	DPRSTP*	PSI*	OPERATION MODE
0	1	1	2-PHASE CCM
0	1	0	1-PHASE CCM
1	0	1	1-PHASE DCM
1	0	0	1-PHASE DCM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0307	1	RES,MTL FILM,1/16W,8.25K,1.0402,SMD,LF	R7417		IMVP6:1PHASE
114S0336	1	RES,MTL FILM,1/16W,16.9K,1.0402,SM,LF	R7416		IMVP6:1PHASE
132S0080	1	CAP,CER,.22UF,20.6.3V,XSR,0402	C7428		IMVP6:1PHASE
114S0236	1	RES,MTL FILM,1/16W,1.58K,1.0402,SMD,LF	R7409		IMVP6:1PHASE
114S0160	1	RES,MTL FILM,1/16W,255 OHM,1.0402,SMD,LF	R7411		IMVP6:1PHASE
132S4720	1	CAP CER 470PF,+/-10%,50V,0402,SMD	C7406		IMVP6:1PHASE
114S0410	1	RES,MTL FILM,1/16W,97.6K,1.0402,SMD,LF	R7414		IMVP6:1PHASE
132S0045	1	CAP,CER,1000PF,50V,10%,X78,0402,SMD	C7414		IMVP6:1PHASE
131S1027	1	CAP,CER,1000PF,5%,50V,CC0402	C7413		IMVP6:1PHASE

REVISION	DATE	BY	CHKD	APP'D	DESCRIPTION
051-8561	11/18/2009				Initial Release

[illegible][illegible][illegible]

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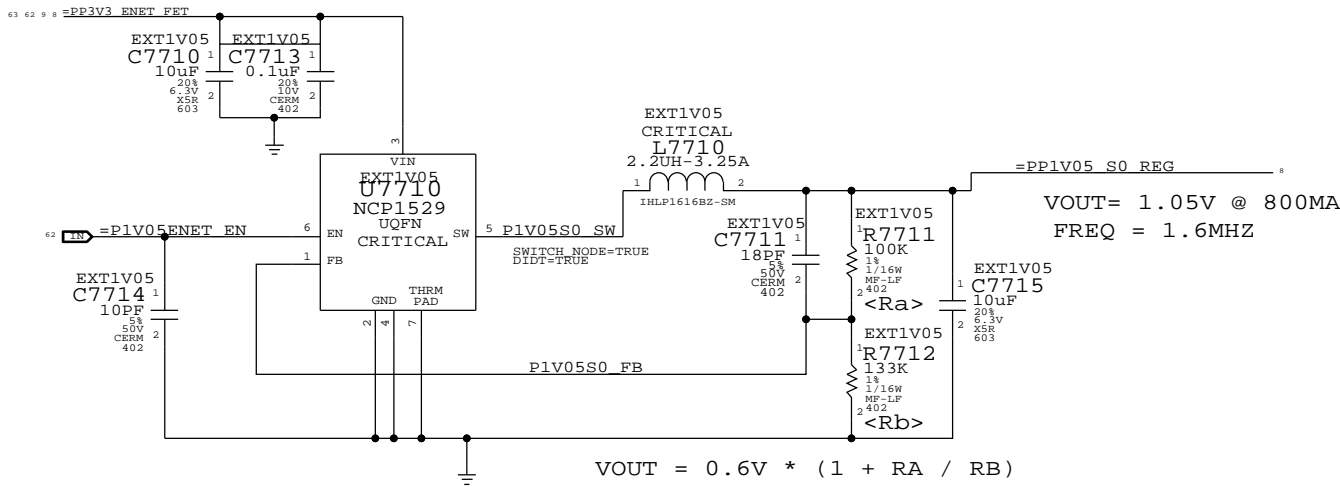
D

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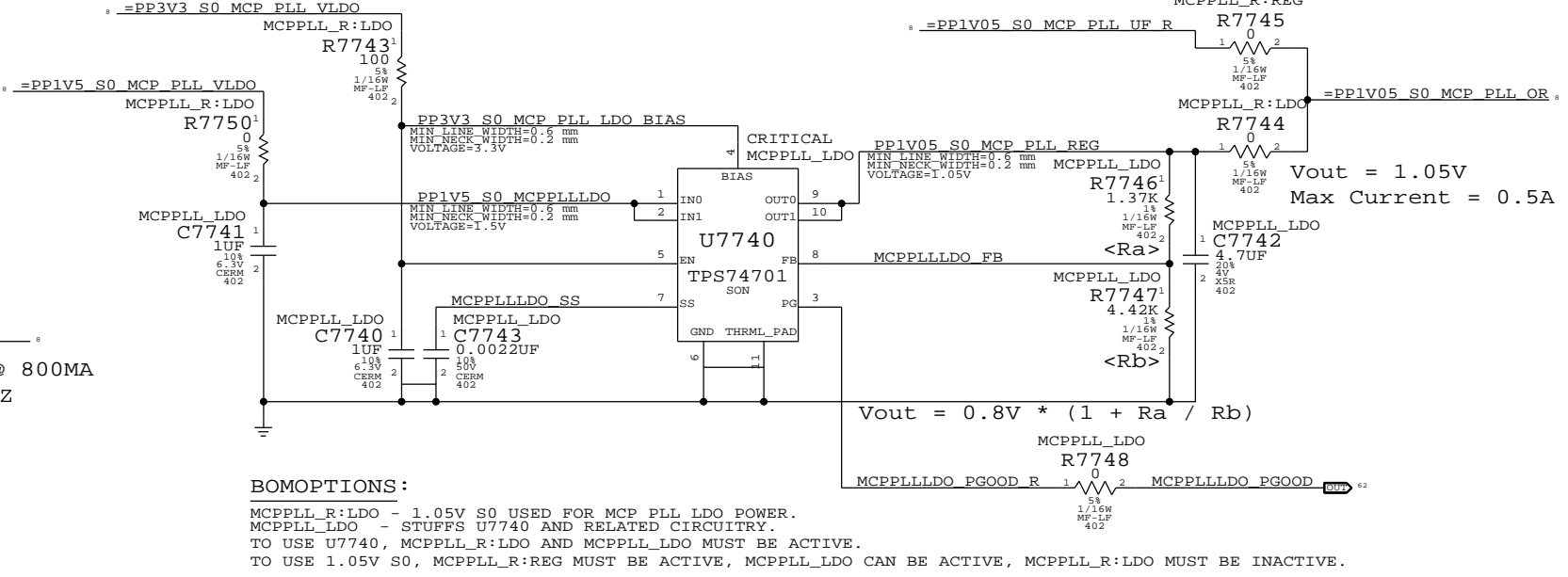
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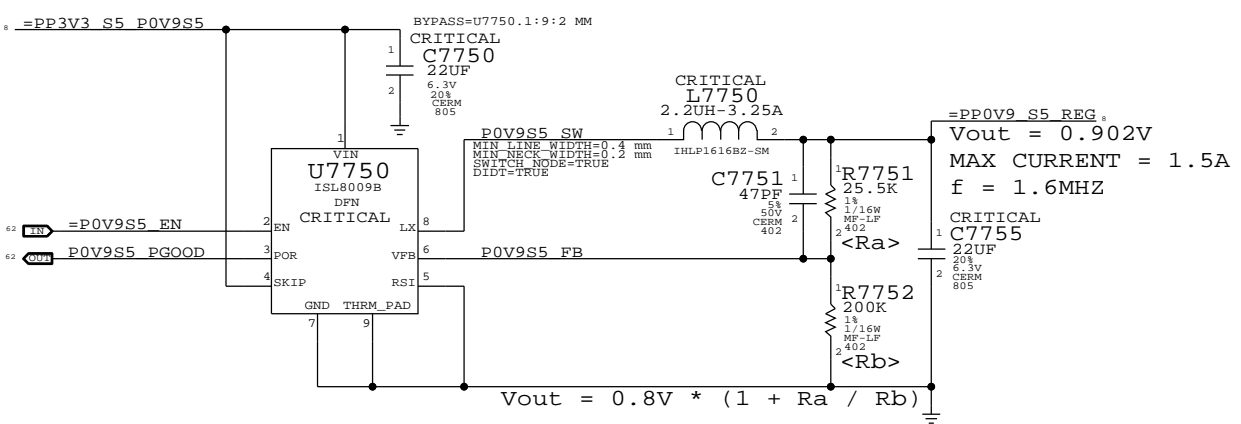
1.05V ENET Switcher



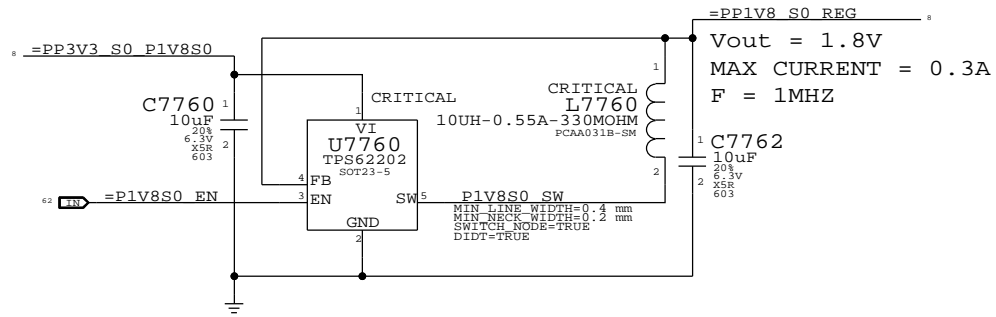
1.05V S0 MCP PLL LDO




MCP 0.9V S5 (AUXC) Switcher



1.8V S0 Switcher



K6 NOTES : C7710 AND C7750 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
Misc Power Supplies			
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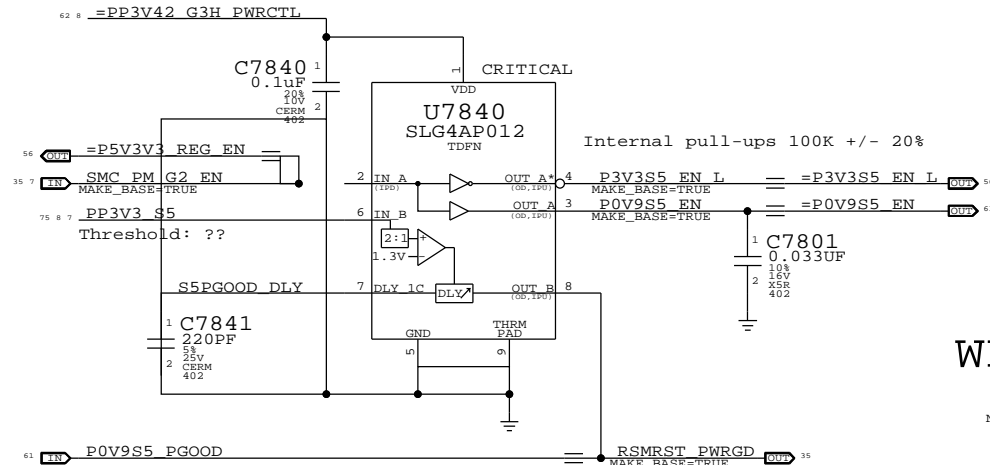
4

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1

S5 Rail Enables & PGOOD

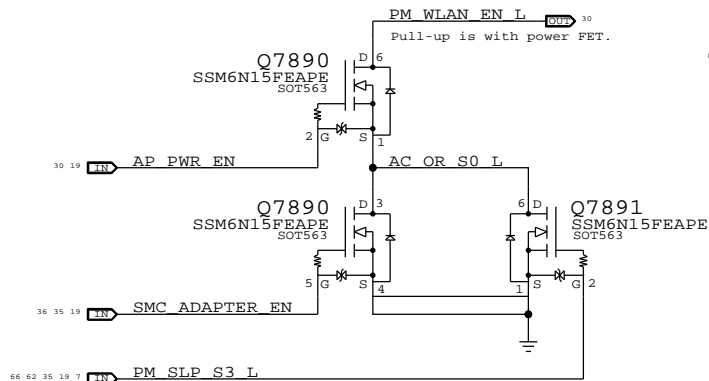


Power Control Signals

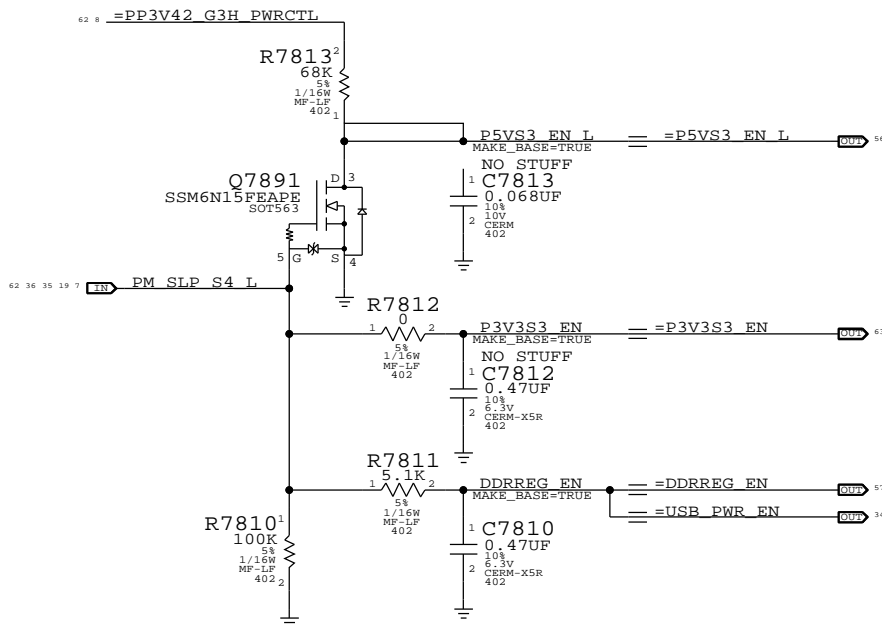
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

WLAN Enable Generation

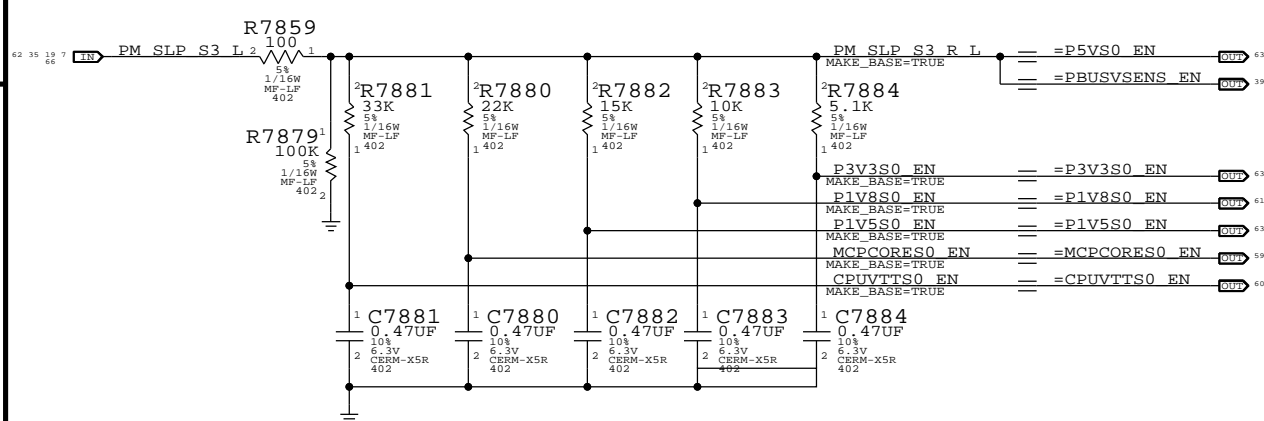
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



S3 Rail Enables



S0 Rail Enables



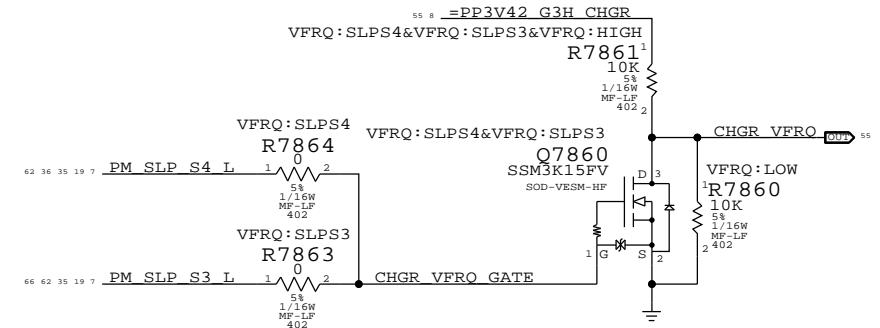
VTT Rail Enable

VTT rail must ramp up in about the same time as MEMVDD rail (Q2300).

DO NOT SYNC T27, ENET RAILS CHANGED

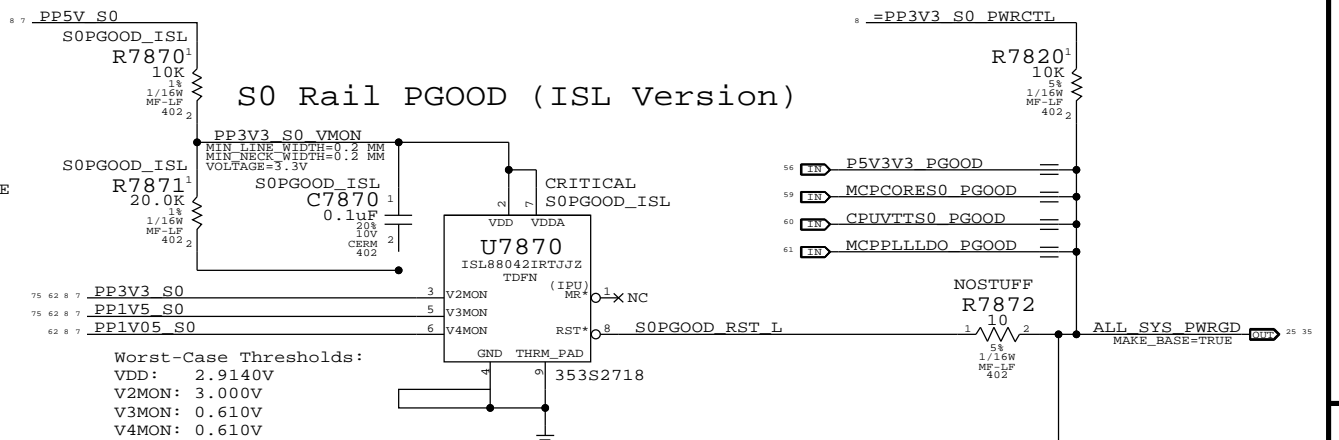
=DDRVT EN

ISL6259 Frequency Select

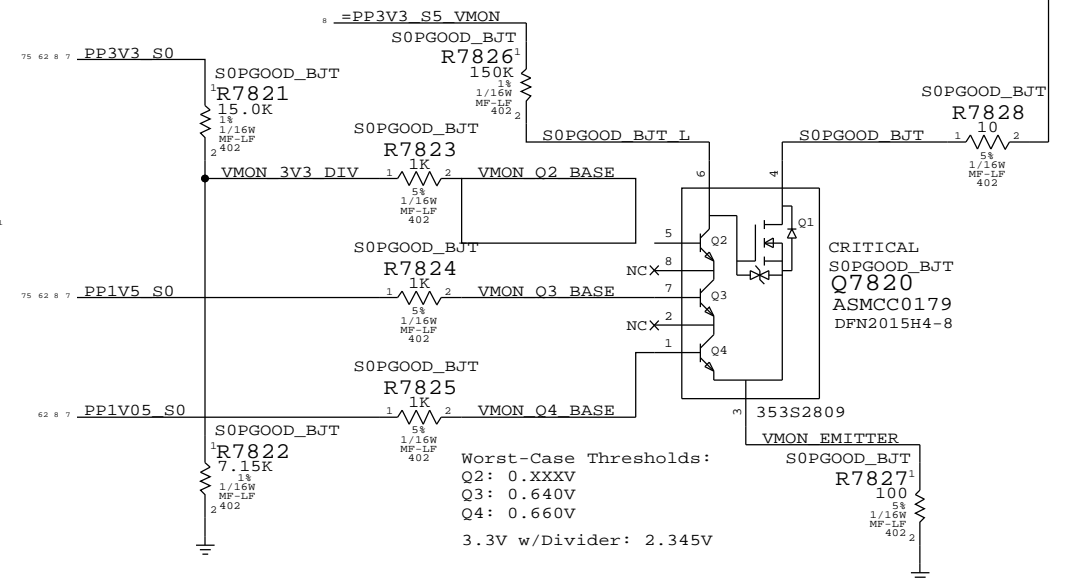


S0 Rail PGOOD Circuitry

S0 Rail PGOOD (ISL Version)



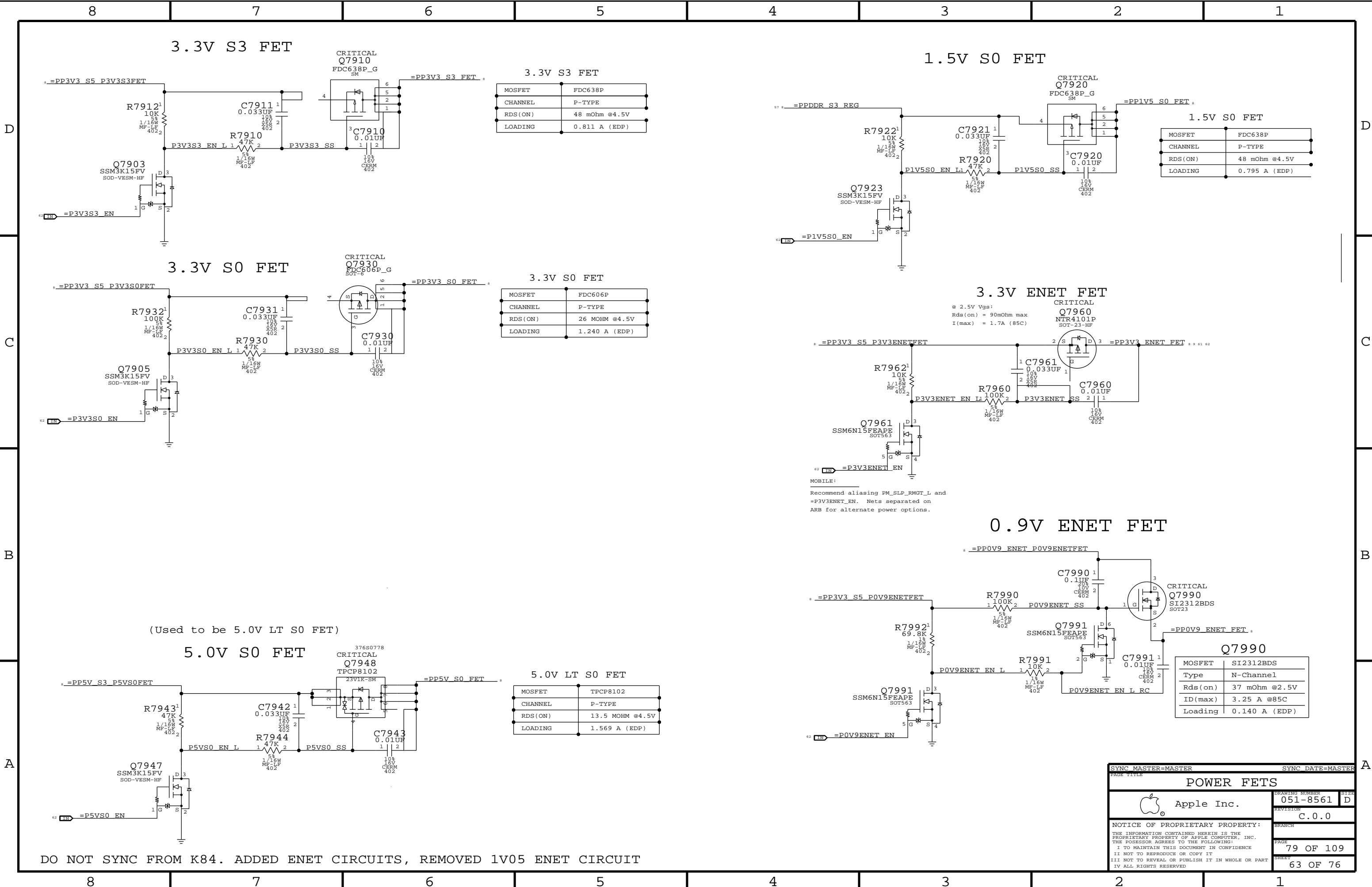
S0 Rail PGOOD (BJT Version)




Unused PGOOD signal

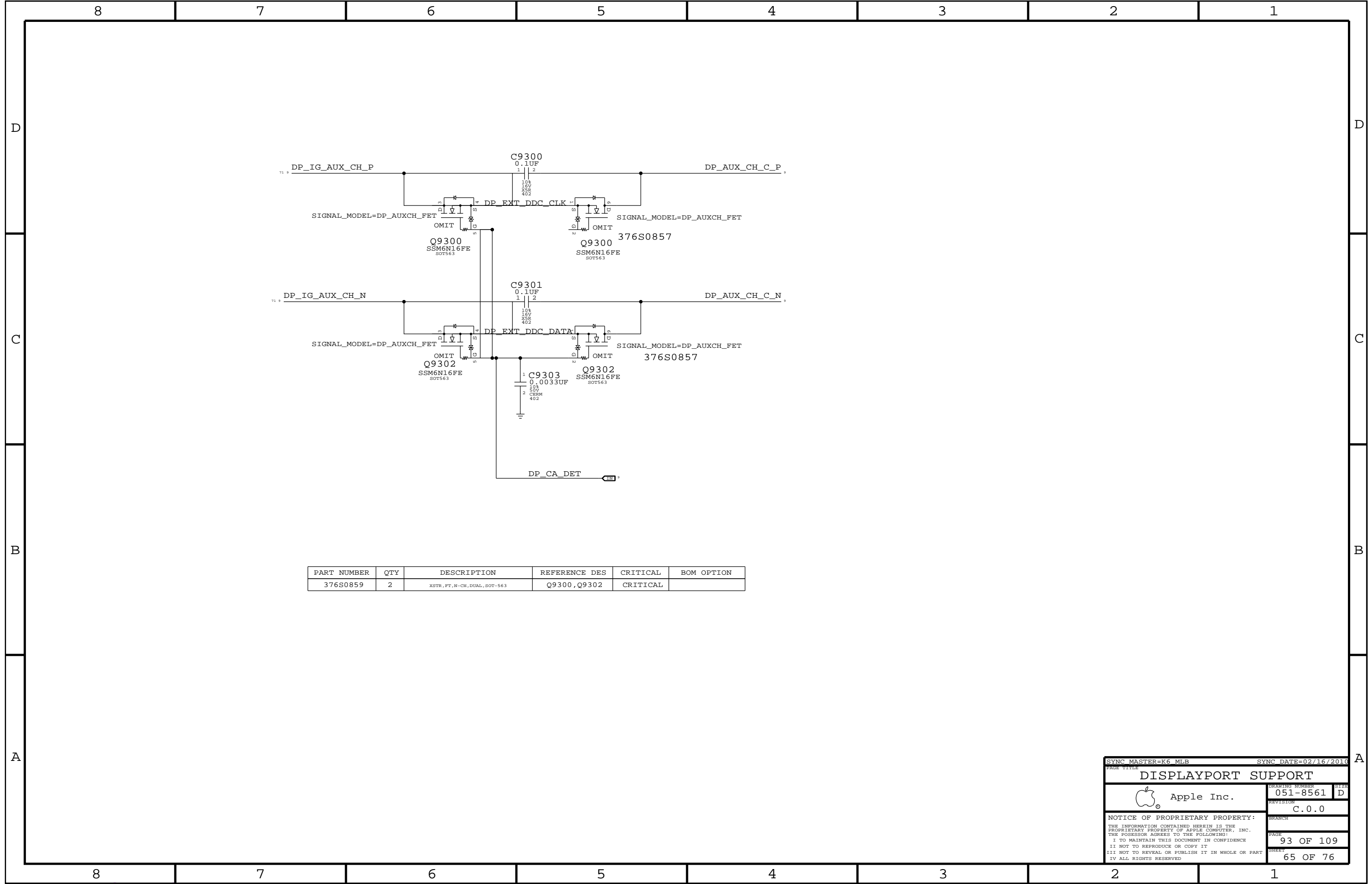
DDRREG_PGOOD = TP_DDRREG_PGOOD

PAGE TITLE		PAGE NUMBER	
Power Sequencing		051-8561	
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DO NOT SYNC FROM K84. ADDED ENET CIRCUITS, REMOVED 1V05 ENET CIRCUIT

SYNC MASTER=MASTER		SYNC DATE=MASTER	
PAGE TITLE			
POWER FETS			
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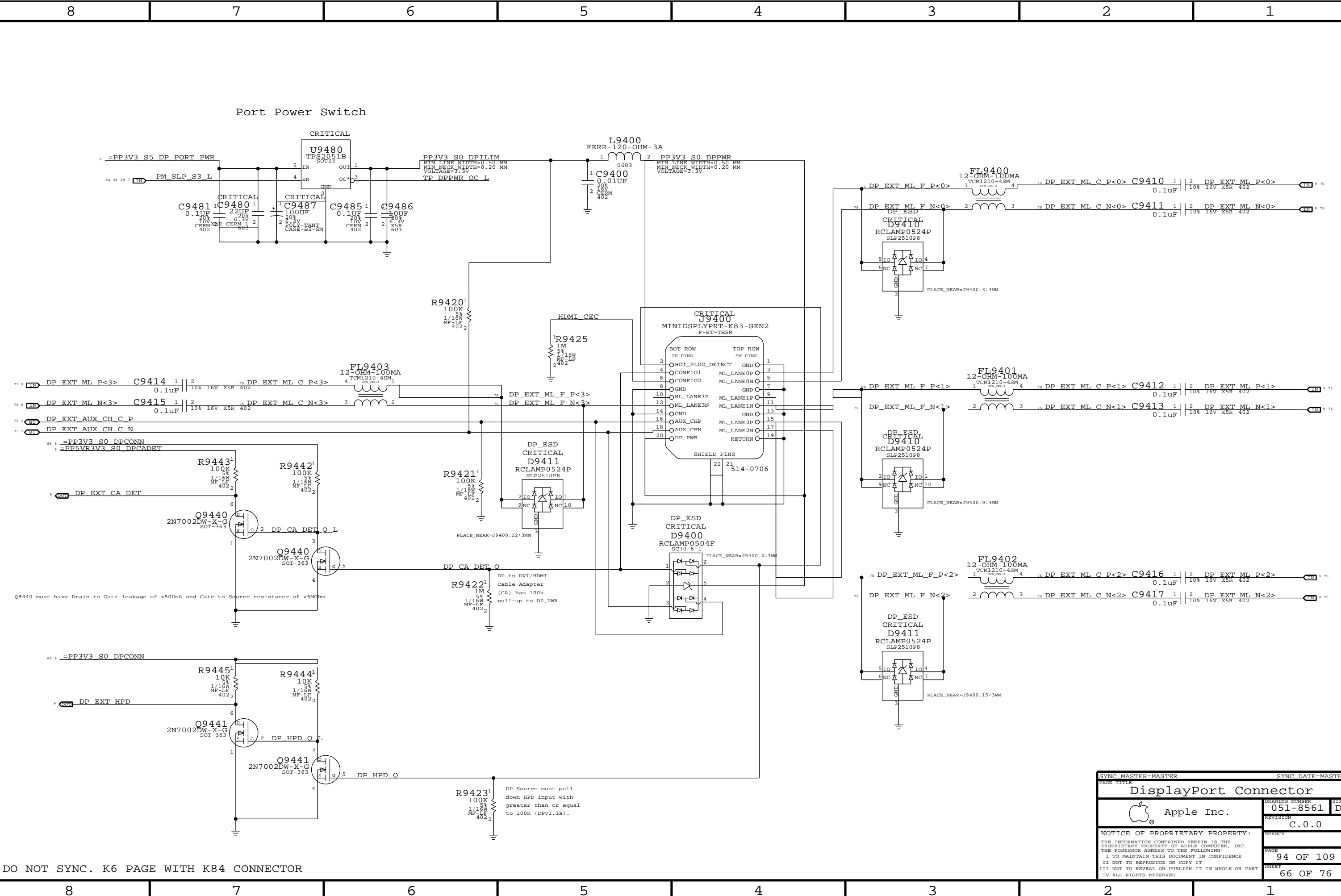
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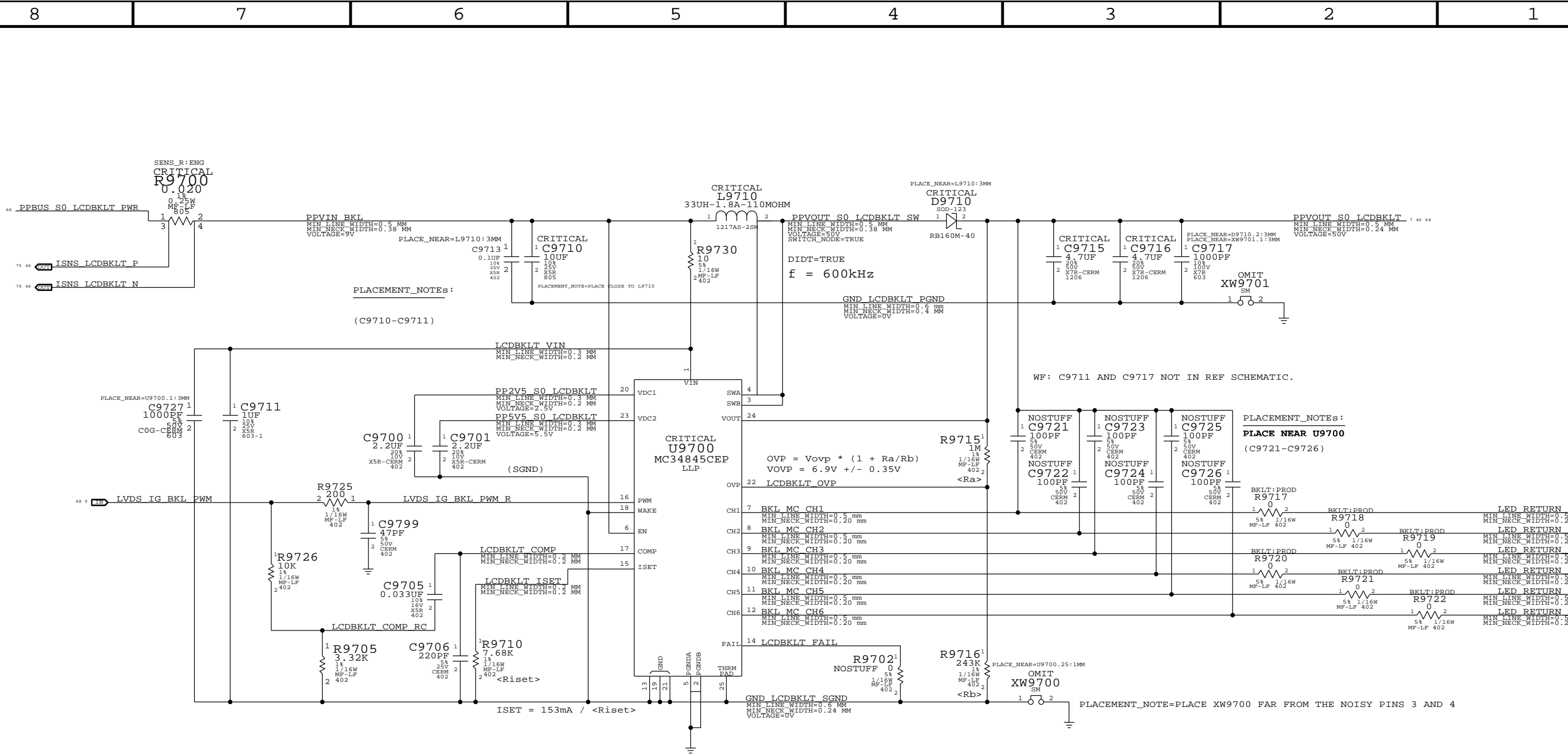
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PAGE TITLE		PAGE TITLE	
DisplayPort Connector		DisplayPort Connector	
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13.3 Inch, K84 Panel (9 LEDs per string)
TARGET: ISET = 20mA, OVP = 35V
ACTUAL: ISET = 19.9mA, OVP = 35.2V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG
101S0075	1	RES,MF,0 OHM,5%,1/8W,SMD,LF,0805	R9700		SENS_R:PROD

10.2 ohm resistors for current measurement on LED strings.

DO NOT SYNC FROM K84. L9710 CHANGED TO K6/K69

SYNC MASTER=MASTER

SYNC DATE=MASTER

LCD Backlight Driver (MC34845)

Apple Inc.

DRAWING NUMBER

051-8561

SIZE

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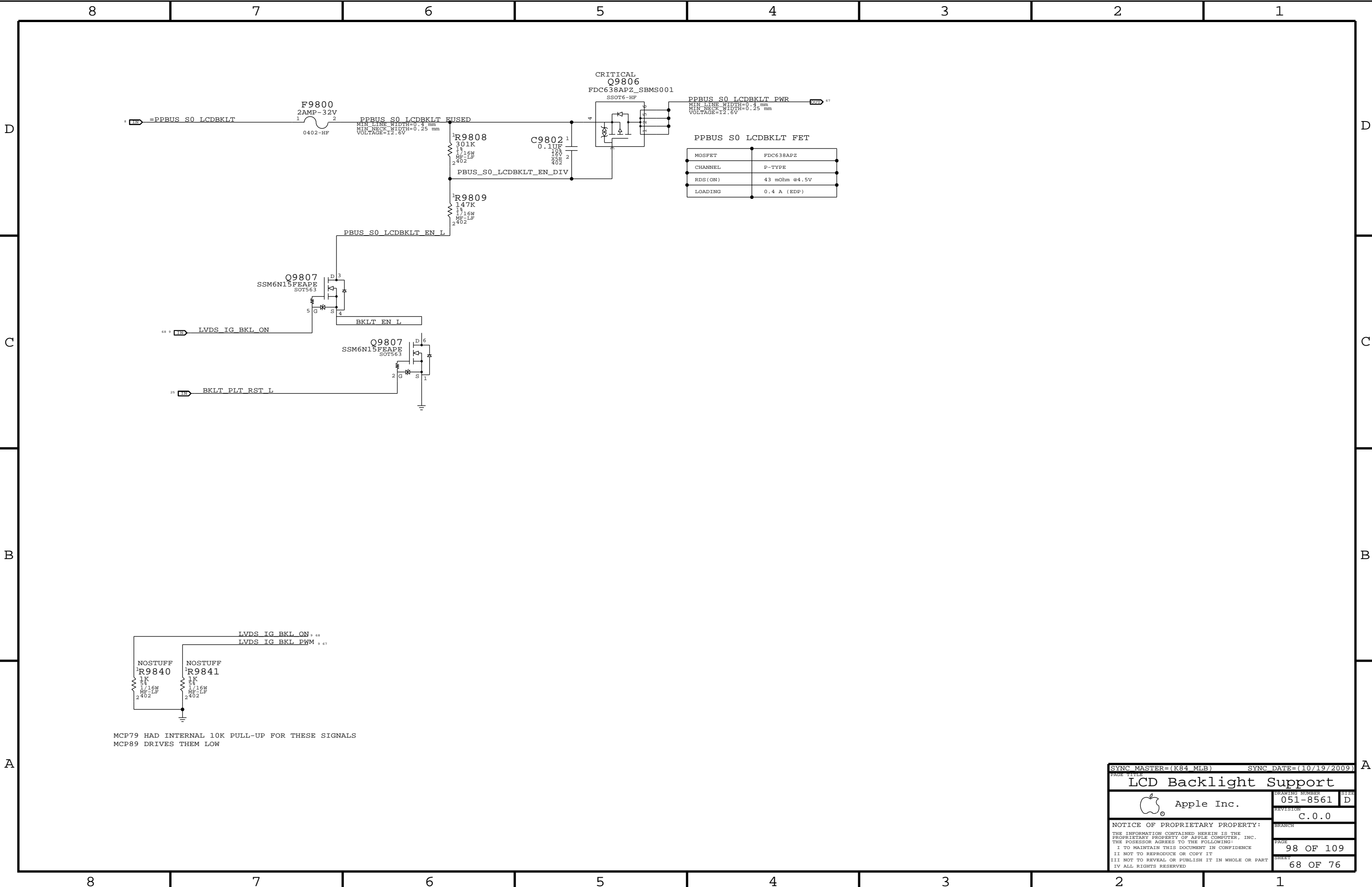
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MCP79 HAD INTERNAL 10K PULL-UP FOR THESE SIGNALS
MCP89 DRIVES THEM LOW

SYNC MASTER=(K84_MLB) SYNC DATE=(10/19/2009)

LCD Backlight Support

 Apple Inc.

DRAWING NUMBER
051-8561

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 135 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 2

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FOR 1K signals shown in signal table on right

FSB 1X signals shown in signal table on right.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCD90 Interview PG (PG 04605 001 of 0 0) Continuation 2 of 2

SOURCE: Santa Rosa Platform DG, Box 0.0 (#20517), Sections 4, 4.5, 5, 8, 2, 4

MCB_FSB_COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_S05	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4

FSB Clock Constraints


[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

		NET TYPE				
		ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	7 10 14	
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	7 10 14	
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	7 10 14	
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	7 10 14	
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	7 10 14	
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	7 10 14	
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	7 10 14	
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	7 10 14	
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	7 10 14	
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	7 10 14	
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	7 10 14	
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	7 10 14	
FSB 2X Signals	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	7 10 14	
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	7 10 14	
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	7 10 14	
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	7 10 14	
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	7 10 14	
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	7 10 14	
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	7 10 14	
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	7 10 14	
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	7 10 14	
	FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB ADS L	7 10 14
		FSB_BREQ0_L	FSB_50S	FSB_1X	FSB BREQ0_L	10 14
		FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10 14
FSB_1X		FSB_50S	FSB_1X	FSB BPRI L	10 14	
FSB_1X		FSB_50S	FSB_1X	FSB DBSY L	10 14	
FSB_1X		FSB_50S	FSB_1X	FSB DEFER L	10 14	
FSB_1X		FSB_50S	FSB_1X	FSB DRDY L	10 14	
FSB_1X		FSB_50S	FSB_1X	FSB HIT L	7 10 14	
FSB_1X		FSB_50S	FSB_1X	FSB HITM L	7 10 14	
FSB_1X		FSB_50S	FSB_1X	FSB LOCK L	7 10 14	
FSB_CPURST_L		FSB_50S	FSB_1X	FSB CPURST L	10 13 14	
FSB_1X		FSB_50S	FSB_1X	FSB RS L<2..0>	10 14	
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10 14		
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M_L	10 14	
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9 10	
	CPU_FERR_L	CPU_50S	CPU_RMIL	CPU FERR_L	10 14	
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNNL	10 14	
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT_L	10 14	
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	10 14	
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	10 14	
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT_L	10 14 36	
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	10 13 14	
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI_L	10 14	
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK_L	10 14	
	PM_THERMTRIP_L	CPU_50S	CPU_RMIL	PM_THERMTRIP_L	10 14 36	
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP_L	10 14		
CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU DPSLP_L	10 14		
CPU_DERSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP_L	10 14 58		
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR_L	10 14		
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU_P	10 14	
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU_N	10 14	
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP_P	13 14	
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP_N	13 14	
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP_P	14	
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP_N	14	
	CPU_IERR_L	CPU_50S		CPU IERR_L	10	
	PM DPRSLPVR	CPU_50S	CPU_AGTL	PM DPRSLPVR	14 58	
	(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLPVR	58	
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK_VML_COMP_VDD	14	
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK_VML_COMP_GND	14	
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU_COMP_VCC	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU_COMP_GND	14		
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10 29	
	CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<3>	10	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10	
	CPU_COMP	CPU_50S	CPU_COMP	CPU COMP<1>	10	
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10	
	XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	10 13	
	XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	10 13	
	XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	10 13	
	XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	10 13	
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST_L	10 13	
	XDP_BFM_L	CPU_50S	CPU_ITP	XDP BFM L<4..0>	10 13	
	XDP_BFM_L5	CPU_50S	CPU_ITP	XDP BFM L<5>	10 13	
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST_L	13		
		CPU_50S	CPU_RMIL	CPU VID<6..0>	11 58	
		CPU_50S	CPU_RMIL	IMVP6 VID<6..0>		
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_P	11 58	
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE_N	11 58	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN_P	58	
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN_N	58	

SYNCH MASTER=T27 MLB		SYNCH DATE=02/16/2010	
PAGE TITLE			
CPU/FSB Constraints			
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		REVISION C.0.0	
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_20OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_20OTHER
MEM_CTRL	*	*	MEM_20OTHER
MEM_CMD	*	*	MEM_20OTHER
MEM_DATA	*	*	MEM_20OTHER
MEM_DQS	*	*	MEM_20OTHER

Need to support MEM_*-style wildcards!

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 360 ps

No DQS to clock matching requirement.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

CMD/CTRL signals should be matched within 150 ps.

All memory signals maximum length is 1.030 ps.

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.3

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

B

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	=2x_DIELECTRIC	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.2.2

A

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK P<5..0>	15 26
MEM_A_CLK	MEM_70D	MEM_CLK	MEM A CLK N<5..0>	15 26
MEM_A_CKE	MEM_40S	MEM_CTRL	MEM A CKE<3..0>	15 21 26
MEM_A_CNTRL	MEM_40S	MEM_CTRL	MEM A CS L<3..0>	15 26
MEM_A_CNTRL	MEM_40S	MEM_CTRL	MEM A ODT<3..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A A<15..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A BA<2..0>	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A RAS L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A CAS L	15 26
MEM_A_CMD	MEM_40S	MEM_CMD	MEM A WE L	15 26
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7>	15 28
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK P<5..0>	15 27
MEM_B_CLK	MEM_70D	MEM_CLK	MEM B CLK N<5..0>	15 27
MEM_B_CKE	MEM_40S	MEM_CTRL	MEM B CKE<3..0>	15 21 27
MEM_B_CNTRL	MEM_40S	MEM_CTRL	MEM B CS L<3..0>	15 27
MEM_B_CNTRL	MEM_40S	MEM_CTRL	MEM B ODT<3..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B A<15..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B BA<2..0>	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B RAS L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B CAS L	15 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM B WE L	15 27
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56>	15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0>	15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1>	15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2>	15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3>	15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4>	15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5>	15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6>	15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0>	15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1>	15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2>	15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3>	15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DOS N<3>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4>	15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5>	15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6>	15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7>	15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7>	15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND	15

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Memory Constraints

Apple Inc.

051-8561

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

NEED PCIe Gen1/Gen2 notes!

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	20 MIL	?
CRT_2CRT	*	15 MIL	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	=4x_DIELECTRIC	?
MCP_DAC_COMP	*	=2x_DIELECTRIC	?

CRT signal single-ended impedance varies by location:

- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.1.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.
NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.
DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max trace length: LVDS 10 inches, DP 8.5 inches.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=3x_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SATA intra-pair matching should be 1 ps.
Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.
SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.6

MCP89 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	PCIE_90D	PCIE	PEG R2D P<15..0>
	PCIE_90D	PCIE	PEG R2D N<15..0>
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>
	PCIE_90D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>
	PCIE_90D	PCIE	PEG D2R N<15..0>
	PCIE_90D	PCIE	PEG D2R C P<15..0>
	PCIE_90D	PCIE	PEG D2R C N<15..0>
	PCIE_90D	PCIE	PCIE AP R2D P
	PCIE_90D	PCIE	PCIE AP R2D N
PCIE_AP_R2D	PCIE_90D	PCIE	PCIE AP R2D C P
	PCIE_90D	PCIE	PCIE AP R2D C N
PCIE_AP_D2R	PCIE_90D	PCIE	PCIE AP D2R P
	PCIE_90D	PCIE	PCIE AP D2R N
	PCIE_90D	PCIE	PCIE ENET R2D P
	PCIE_90D	PCIE	PCIE ENET R2D N
PCIE_ENET_R2D	PCIE_90D	PCIE	PCIE ENET R2D C P
	PCIE_90D	PCIE	PCIE ENET R2D C N
PCIE_ENET_D2R	PCIE_90D	PCIE	PCIE ENET D2R P
	PCIE_90D	PCIE	PCIE ENET D2R N
	PCIE_90D	PCIE	PCIE ENET D2R C P
	PCIE_90D	PCIE	PCIE ENET D2R C N
	PCIE_90D	PCIE	PCIE FW R2D P
	PCIE_90D	PCIE	PCIE FW R2D N
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE FW R2D C P
	PCIE_90D	PCIE	PCIE FW R2D C N
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE FW D2R P
	PCIE_90D	PCIE	PCIE FW D2R N
	PCIE_90D	PCIE	PCIE FW D2R C P
	PCIE_90D	PCIE	PCIE FW D2R C N
MCP_PE0_BEECLK	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P
	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N
MCP_PE1_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP N
MCP_PE2_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M ENET N
MCP_PE3_BEECLK	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P
	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX0_TERM
CRT_RED	CRT_50S	CRT	CRT IG R C PR
CRT_GREEN	CRT_50S	CRT	CRT IG G Y Y
CRT_BLUE	CRT_50S	CRT	CRT IG B COMP PB
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC
CRT_SYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC P
TMDS_IG_TXC	DP_90D	DISPLAYPORT	TMDS IG TXC N
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD P<5..0>
TMDS_IG_TXD	DP_90D	DISPLAYPORT	TMDS IG TXD N<5..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML P<3..0>
DP_EXT_ML	DP_90D	DISPLAYPORT	DP IG ML N<3..0>
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH P
DP_EXT_AUX_CH	DP_90D	DISPLAYPORT	DP IG AUX CH N
MCP_TMDS0_RSET	MCP_DV_COMP		MCP_TMDS0_RSET
MCP_TMDS0_VPROBE			MCP_TMDS0_VPROBE
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK P
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS IG A CLK N
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA P<3>
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS IG A DATA N<3>
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK P
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS IG B CLK N
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA P<3>
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS IG B DATA N<3>
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE
SATA_HDD_R2D	SATA_90D	SATA	SATA HDD R2D C P
	SATA_90D	SATA	SATA HDD R2D C N
	SATA_90D	SATA	SATA HDD R2D P
	SATA_90D	SATA	SATA HDD R2D N
SATA_HDD_D2R	SATA_90D	SATA	SATA HDD D2R P
	SATA_90D	SATA	SATA HDD D2R N
	SATA_90D	SATA	SATA HDD D2R C P
	SATA_90D	SATA	SATA HDD D2R C N
SATA_ODD_R2D	SATA_90D	SATA	SATA ODD R2D C P
	SATA_90D	SATA	SATA ODD R2D C N
	SATA_90D	SATA	SATA ODD R2D P
	SATA_90D	SATA	SATA ODD R2D N
SATA_ODD_D2R	SATA_90D	SATA	SATA ODD D2R P
	SATA_90D	SATA	SATA ODD D2R N
	SATA_90D	SATA	SATA ODD D2R C P
	SATA_90D	SATA	SATA ODD D2R C N
MCP_SATA_TERM		SATA_TERM	MCP_SATA_TERM

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PAGE TITLE

MCP Constraints 1

Apple Inc.

DRAWING NUMBER

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MIL_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MIL_555	*	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=55_OHM_SR	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?


























SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

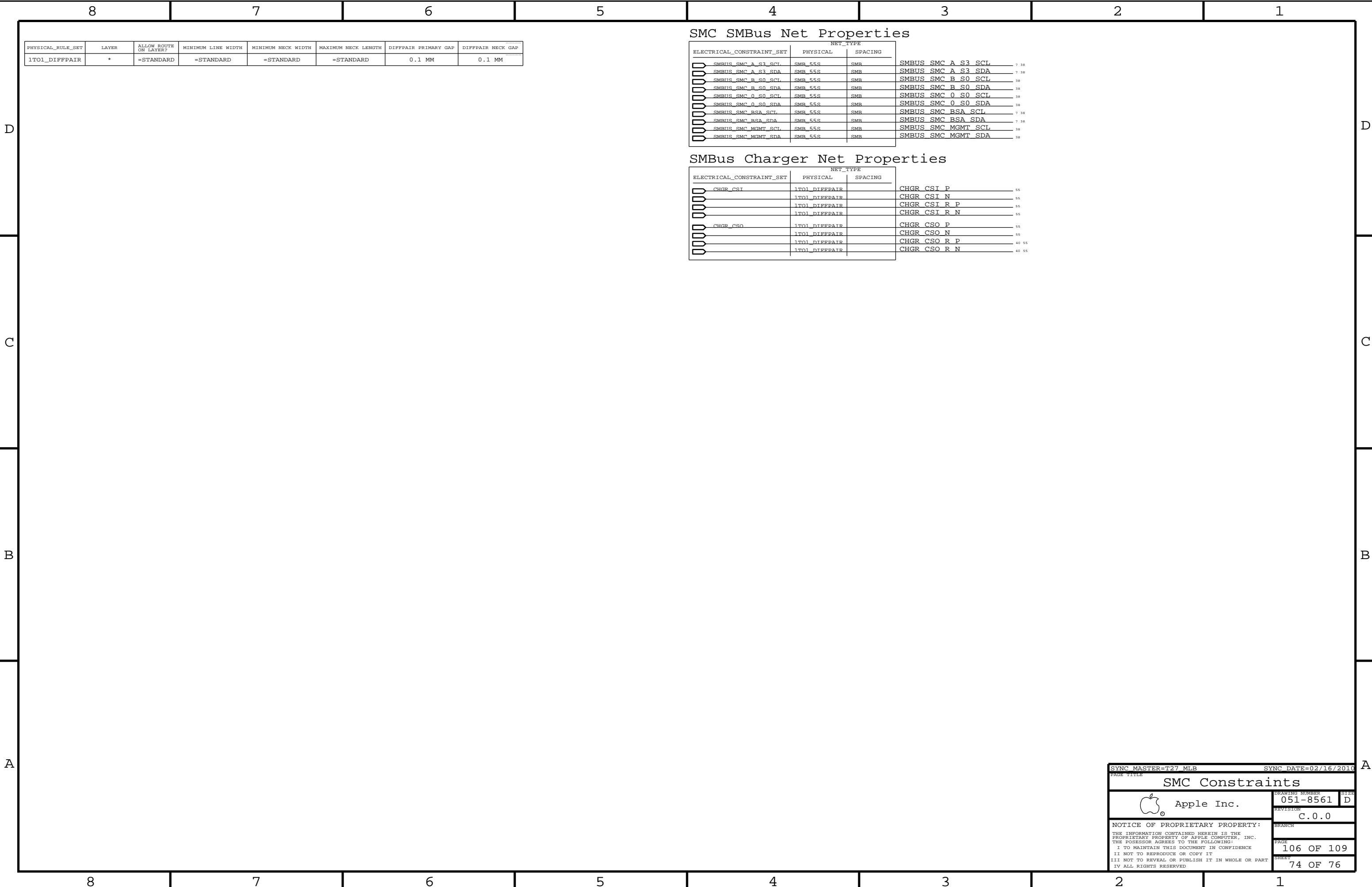
88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENRY_MDI_100D	*	<100_OHM_DIFF	>100_OHM_DIFF	>100_OHM_DIFF	>100_OHM_DIFF	>100_OHM_DIFF	>100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENHET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET		SET_TYPE		
		PHYSICAL	SPACING	
	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD 18
	MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND 18
	MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M BUF0 R 9
		ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1 31
	ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET INTR L 18
	ENET_MDIO	ENET_MII_55S	ENET_MII	ENET MDIO 31 31
	ENET_MDC	ENET_MII_55S	ENET_MII	ENET MDC 9 31
	ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET PWRDWN L 18
		ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK R 31
	ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK 31 31
		ENET_MII_55S	ENET_MII	ENET RXD R<3..0> 31
	ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET RXD<0> 31 31
	ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET RXD<3..1> 18 31
	ENET_RXD	ENET_MII_55S	ENET_MII	ENET RX CTRL 18 31
		ENET_MII_55S	ENET_MII	ENET RXCTL R 31
		ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK R 31
	ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK 9 31
	ENET_TXD0	ENET_MII_55S	ENET_MII	ENET TXD<0> 9 31
	ENET_TXD	ENET_MII_55S	ENET_MII	ENET TXD<3..1> 9 31
	ENET_TXD	ENET_MII_55S	ENET_MII	ENET TX CTRL 9 31
		ENET_MII_55S	ENET_MII	ENET RESET L 9 31
	ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0> 31 32
		ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0> 31 32
		ENET_MDI_100D	ENET_MDI	ENET MDI TRAN P<3..0> 31 32
		ENET_MDI_100D	ENET_MDI	ENET MDI TRAN N<3..0> 32



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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
MEM_POWER	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_POWER	*	PWR_P2MM
MEM_CMD	MEM_POWER	*	PWR_P2MM
MEM_CTRL	MEM_POWER	*	PWR_P2MM
MEM_DATA	MEM_POWER	*	PWR_P2MM
MEM_DQS	MEM_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

MCP Fanout Constraint Relaxations

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	*	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	*	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE

Misc Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	(PCIE_AP)	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP CONN P
		CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M AP CONN N
	(USB_EXT_A)	USB_90D	USB	USB_EXT_A MIXED P
	(USB_EXT_A)	USB_90D	USB	USB_EXT_A MIXED N
	(USB_EXT_A)	USB_90D	USB	USB LT1 P
	(USB_EXT_A)	USB_90D	USB	USB LT1 N
	(USB_TPAD)	USB_90D	USB	USB_TPAD_R_P
	(USB_TPAD)	USB_90D	USB	USB_TPAD_R_N
	(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P
	(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N
		USB_90D	USB	USB_LT2_P
		USB_90D	USB	USB_LT2_N
		ENET_MDIO_100D	ENETCONN	ENETCONN_P<3..0>
		ENET_MDIO_100D	ENETCONN	ENETCONN_N<3..0>
		SATA_90D	SATA	SATA_ODD_R2D_UF_P
		SATA_90D	SATA	SATA_ODD_R2D_UF_N
		SATA_90D	SATA	SATA_ODD_D2R_UF_P
		SATA_90D	SATA	SATA_ODD_D2R_UF_N
		SATA_90D	SATA	SATA_HDD_D2R_FILT_P
		SATA_90D	SATA	SATA_HDD_D2R_FILT_N
		SATA_90D	SATA	SATA_HDD_D2R_UF_P
		SATA_90D	SATA	SATA_HDD_D2R_UF_N
		SATA_90D	SATA	SATA_HDD_R2D_UF_P
		SATA_90D	SATA	SATA_HDD_R2D_UF_N
		SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_P
		SATA_90D	SATA	SATA_HDD_D2R_RDRV_IN_N
		SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_P
		SATA_90D	SATA	SATA_HDD_R2D_RDRV_IN_N
		SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_P
		SATA_90D	SATA	SATA_HDD_D2R_RDRV_OUT_N
		SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_P
		SATA_90D	SATA	SATA_HDD_R2D_RDRV_OUT_N
		SATA_90D	SATA	SATA_HDD_D2R_NORDRV_P
		SATA_90D	SATA	SATA_HDD_D2R_NORDRV_N
		SATA_90D	SATA	SATA_HDD_R2D_NORDRV_P
		SATA_90D	SATA	SATA_HDD_R2D_NORDRV_N
	PCIE_AP_D2R	PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_P
		PCIE_90D	PCIE	CONN_PCIE_MINI_D2R_N
	PCIE_AP_R2D	PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_P
		PCIE_90D	PCIE	CONN_PCIE_MINI_R2D_N
	USB_BT	USB_90D	USB	CONN_USB2_BT_P
		USB_90D	USB	CONN_USB2_BT_N
	LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P
		LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N
	MCP_PEL_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P
		CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N
USB	USB_EXT_A	USB_90D	USB	CONN_USB_EXT_A_P
USB		USB_90D	USB	CONN_USB_EXT_A_N
USB	USB_EXT_B	USB_90D	USB	CONN_USB_EXT_B_P
USB		USB_90D	USB	CONN_USB_EXT_B_N

Power Net Properties


ELECTRICAL_CONSTRAINT_SET		NET TYPE		
		PHYSICAL	SPACING	
	CPU1THMSNS_D2	THERM 1T01 55S	THERM	CPUTHMSNS D1 P 41
		THERM 1T01 55S	THERM	CPUTHMSNS D1 N 41
RES	CPU1THMSNS_D2	THERM 1T01 55S	THERM	CPUTHMSNS D2 P 41
RES		THERM 1T01 55S	THERM	CPUTHMSNS D2 N 41
	CPU1 THERMD	THERM 1T01 55S	THERM	CPU THERMD P 10 41
		THERM 1T01 55S	THERM	CPU THERMD N 10 41
	MCPTHMSNS_D2	THERM 1T01 55S	THERM	MCPTHMSNS D2 P
		THERM 1T01 55S	THERM	MCPTHMSNS D2 N
	MCP_THMDIODE	THERM 1T01 55S	THERM	MCP THMDIODE P 19 41
		THERM 1T01 55S	THERM	MCP THMDIODE N 19 41
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS 1V5 S3 P
		SENSE 1T01 55S	SENSE	ISNS 1V5 S3 N
		SENSE 1T01 55S	SENSE	ISNS 1V5 S3 R P
		SENSE 1T01 55S	SENSE	ISNS 1V5 S3 R N
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS AIRPORT P 30 46
		SENSE 1T01 55S	SENSE	ISNS AIRPORT N 30 46
		SENSE 1T01 55S	SENSE	ISNS AIRPORT R P 46
		SENSE 1T01 55S	SENSE	ISNS AIRPORT R N 46
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS HDD P 33 46
		SENSE 1T01 55S	SENSE	ISNS HDD N 33 46
		SENSE 1T01 55S	SENSE	ISNS HDD R P 46
		SENSE 1T01 55S	SENSE	ISNS HDD R N 46
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS LCDBKLT P 46 67
		SENSE 1T01 55S	SENSE	ISNS LCDBKLT N 46 67
		SENSE 1T01 55S	SENSE	ISNS LCDBKLT R P
		SENSE 1T01 55S	SENSE	ISNS LCDBKLT R N
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS ODD P 33 46
		SENSE 1T01 55S	SENSE	ISNS ODD N 33 46
		SENSE 1T01 55S	SENSE	ISNS ODD R P 46
		SENSE 1T01 55S	SENSE	ISNS ODD R N 46
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	ISNS CPUVTT P 40
		SENSE 1T01 55S	SENSE	ISNS CPUVTT N 40
	SENSE_DIFFPAIR	SENSE 1T01 55S	SENSE	MCPCORES0 VSEN P 22 59
		SENSE 1T01 55S	SENSE	MCPCORES0 VSEN N 22 59
		MEM_POWER		PP1V5R1V35 S3 7 8
		SB_POWER		PP3V3 S5 7 8 62
		SB_POWER		PP3V3 S0 7 8 62
		SB_POWER		PP1V5 S0 7 8 62
		GND		GND

Audio Net Properties

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
		DIFFPAIR	AUDIO	AUD SPKRAMP LIN P
		DIFFPAIR	AUDIO	AUD SPKRAMP LIN N
		DIFFPAIR	AUDIO	AUD SPKRAMP SUBIN P
		DIFFPAIR	AUDIO	AUD SPKRAMP SUBIN N
		DIFFPAIR	AUDIO	AUD SPKRAMP RIN P
		DIFFPAIR	AUDIO	AUD SPKRAMP RIN N
		DIFFPAIR	AUDIO	SSM2315L P
		DIFFPAIR	AUDIO	SSM2315L N
		DIFFPAIR	AUDIO	SSM2315S P
		DIFFPAIR	AUDIO	SSM2315S N
		DIFFPAIR	AUDIO	SSM2315R P
		DIFFPAIR	AUDIO	SSM2315R N
	SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN L OUT P
		DIFFPAIR	AUDIO	SPKRCONN L OUT N
	SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN S OUT P
		DIFFPAIR	AUDIO	SPKRCONN S OUT N
	SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN R OUT P
		DIFFPAIR	AUDIO	SPKRCONN R OUT N
		DIFFPAIR	AUDIO	BI MIC P
		DIFFPAIR	AUDIO	BI MIC N
		DIFFPAIR	AUDIO	HS MIC P
		DIFFPAIR	AUDIO	HS MIC N

GRAPHICS NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
(DP_EXT_ML)	DP_90D	DISPLAYPORT	DP EXT ML P<3..0> 9 66
	DP_90D	DISPLAYPORT	DP EXT ML N<3..0> 9 66
	DP_90D	DISPLAYPORT	DP EXT ML C P<3..0> 66
	DP_90D	DISPLAYPORT	DP EXT ML C N<3..0> 66
	DP_90D	DISPLAYPORT	DP EXT ML F P<3..0> 66
	DP_90D	DISPLAYPORT	DP EXT ML F N<3..0> 66
(DP_EXT_AUX_CH)	DP_90D	DISPLAYPORT	DP EXT AUX CH C P 9 66
	DP_90D	DISPLAYPORT	DP EXT AUX CH C N 9 66
	DP_90D	DISPLAYPORT	DP EXT DDC DATA 65
	DP_90D	DISPLAYPORT	DP EXT DDC CLK 65

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K87 SPECIFIC CONSTRAINTS			
 Apple Inc.		DRAWING NUMBER 051-8561	SIZE D
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K87 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS							
BOARD LAYERS				BOARD AREAS		BOARD UNITS (MIL, OZ, MM)	ALLEGRO VERSION
TOP, 10L2, 10L3, 10L4, 10L5, 10L6, 10L7, 10L8, 10L9, 10L10, 10L11, BOTTOM				BG_TYPES, BGA_P10M		MM	16.5.1
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	<50_OHM_SE	0.100MM	30 MM	0 MM	0 MM
STANDARD	*	Y	<DEFAULT	<DEFAULT	12.7 MM	<DEFAULT	<DEFAULT
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	<STANDARD	<STANDARD	<STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.115 MM	0.115 MM			
50_OHM_SE	*	Y	0.076 MM	0.076 MM	<STANDARD	<STANDARD	<STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.100 MM			
40_OHM_SE	*	Y	0.126 MM	0.100 MM	<STANDARD	<STANDARD	<STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	*	Y	0.222 MM	0.222 MM	<STANDARD	<STANDARD	<STANDARD
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
70_OHM_DIFF	10L3, 10L4, 10L9, 10L10	Y	0.151 MM	0.100 MM	<STANDARD	0.224 MM	0.224 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.100 MM		0.200 MM	0.200 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
90_OHM_DIFF	10L3, 10L4, 10L9, 10L10	Y	0.095 MM	0.095 MM		0.234 MM	0.234 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.112 MM	0.112 MM		0.220 MM	0.220 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	<STANDARD	<STANDARD	<STANDARD	<STANDARD	<STANDARD
100_OHM_DIFF	10L3, 10L4, 10L9, 10L10	Y	0.075 MM	0.075 MM		0.244 MM	0.244 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.091 MM	0.091 MM		0.230 MM	0.230 MM
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1+1_DIFFPAIR	*	Y	<STANDARD	<STANDARD	<STANDARD	0.1 MM	0.1 MM
SPACING_RULE_SET							
LAYER							
LINE-TO-LINE SPACING							
WEIGHT							
DEFAULT							
*							
0.1 MM							
?							
STANDARD							
*							
<DEFAULT							
?							
BGA_P10M							
*							
<DEFAULT							
?							
BGA_P20M							
*							
<DEFAULT							
?							
BGA_P30M							
*							
<DEFAULT							
?							
BGA_P10M							
NET_SPACING_TYPE1							
NET_SPACING_TYPE2							
AREA_TYPE							
SPACING_RULE_SET							
*							
*							
BGA_P10M							
BGA_P10M							
MEM_CLK							
*							
BGA_P10M							
BGA_P20M							
CLK_FSB							
*							
BGA_P10M							
BGA_P20M							
CLK_LPC							
*							
BGA_P10M							
BGA_P20M							
CLK_PCIE							
*							
BGA_P10M							
BGA_P20M							
CLK_SLOW							
*							
BGA_P10M							
BGA_P20M							
FSB_DSTB							
FSB_DSTB							
BGA_P10M							
BGA_P30M							
NET_PHYSICAL_TYPE							
AREA_TYPE							
PHYSICAL_RULE_SET							
MEM_400							
BGA_P10M							
STANDARD							
SYNC_MASTER=MASTER							
SYNC_DATE=MASTER							
PAGE TITLE							
K87 RULE DEFINITIONS							
DRAWING NUMBER							
051-8561							
SIZE							
D							
REVISION							
C.0.0							
BRANCH							
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